Thermoelectric devices: Silicon as a possible construction material

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Ágrip:

Markmið verkefnisins var að smíða tæki sem breytt getur varmaorku beint í rafmagn (thermoelectric device).

Slík tæki eru vel þekkt en virkni þeirra byggir á svonefndum Seebeck-hrifum. Hönnunarskilyrði var að virka efnið í tækinu yrði úr kísli (Si).

Byrjað var með kísilskífur af mismunandi leiðnigerð, rafleiðandi og holuleiðandi, sem skornar voru niður og tengdar saman. Verkefnið var unnið við Örtæknikjarna sem staðsettur er í einni af byggingum Háskóla Íslands og er í sameiginlegri eigu Háskóla Íslands, Háskólans í Reykjavík og Nýsköpunarmiðstöðvar Íslands. Afrakstur verkefnisins var tæki sem framleitt getur beint mælanlega rafspennu við hitun. Tækið má hita með ýmsum hætti, svo sem með ljósgleypni, heitum vökva eða hitahellu.

Niðurstöður verkefnins munu síðan verða liður í áframhaldandi rannsóknum leiðbeinanda og nemanda á hitaörvaðri rafmagnsframleiðslu.

Verkefnið var unnið með styrk frá Orkurannsóknarsjóði Landsvirkjunnar

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Formáli

Þessi skýrsla er unnin sem lokaverkefni til B.Sc. gráðu í rafmagnstæknifræði við Háskólann í Reykjavík. Gerð verkefnisins fór fram í Örtæknikjarna sem staðsettur er í byggingu VR-3 við Háskóla Íslands. Örtæknikjarninn er í sameiginlegri eigu HÍ, HR og Nýsköpunarmiðstöðvar Íslands. Hugmyndin að verkefninu þróaðist eftir samtöl við Halldór Guðfinn Svavarsson, dósent við Háskólann í Reykjavík og er ætlunin að halda áfram rannsóknum á kísli eftir að B.Sc. gráðu hefur verið lokið.

Verkefnið fjallar um aðferð sem hægt er að beita til að breyta varmaorku í raforku með Seebeck hrifum. Þessi tæki eru þekkt og var ákveðið að skoða notkun kísils við gerð slíkra tækja. Kísill hefur rafeiginleika sem gerir hann kjörinn í slíka vinnslu, en á móti kemur að varmaleiðnieiginleikar hans eru ekki sem best verður á kosið. Rannsóknir hafa hins vegar sýnt fram á að kísill með yfirborð mótað á nanó stærðarbili hefur enn sína góðu rafeiginleika ásamt því að hafa stórbætta varmaleiðnieiginleika og gerir því áframhaldandi rannsóknir mjög spennandi.

Höfundur vill þakka öllum er komu að verkefninu og veittu aðstoð; Einar Örn Sveinbjörnsson, prófessor í eðlisfræði við HÍ, fyrir ótal samtöl um kísil og eiginleika hans og Seyedmohammad Shayestehaminzadeh, Ph.D. nemi við HÍ, Anna Eden Kossoy, nýdoktor við HÍ, Pauline Renaux, Ph.D. nemi við HÍ, og Einar Baldur Þorsteinsson, B.Sc. í eðlisfræði, fyrir aðstoð við búnað og ýmsar sérmælingar. Höfundur vill einnig þakka Halldóri G. Svavarssyni sérstaklega fyrir að hafa vakið áhuga hans á viðfangsefninu og gefið honum tækifæri til að koma sér inn í þessar rannsóknir, sem eru svo ólíkar því er höfundur hefur áður kynnst.

Sérstakar þakkir fær Landsvirkjun fyrir styrk sinn úr Orkurannsóknarsjóði til handa þessu verkefni svo og framtíðar rannsóknum.

Þetta er tileinkað syni mínum, Styrmi Loga Birgissyni. Ég geri þetta allt fyrir þig.

Birgir Hrafn Hallgrímsson

Preface

This report is the final part of a B.Sc. degree in electrical engineering at Reykjavík University. The research in this project was made at the Nanocenter lab in VR-3 located at the University of Iceland. The Nanocenter lab is collaboratively owned by Reykjavík University (RU), University of Iceland (UI) and the Innovation Center of Iceland. The idea for the project came after discussions with Halldór Guðfinnur Svavarsson, associate professor at RU. The plan is to use this project as a stepping stone for masters study on silicon after completing the B.Sc. degree.

The project is about methods which can be used to convert thermal energy to electrical energy with the Seebeck effect. These devices are well known and this project focuses on the use of silicon to construct such devices. Silicon has electrical properties which make it ideal for such uses. However its thermal properties are not ideal. Researchers have however shown that nanoscale structures on a silicon surface still has good electrical qualities as well as greatly improved thermal conduction properties, which makes continued research into the matter an exciting option.

The author would like to thank everyone who helped with the project along the way; Einar Örn Sveinbjörnsson, professor of physics at UI, for countless conversations on silicon and its properties. Anna Eden Kossoy, postdoc at UI, Seyedmohammad Shayestehaminzadeh, Ph.D. student at UI, Pauline Renaux, Ph.D. student at UI, and Einar Baldur Þorsteinsson, B.Sc. physics, for various assistance around the lab and conversations about the subject. The author would also like to thank Halldór G. Svavarsson especially for sparking an interest in the subject and for giving him the opportunity to come into the field, which is so very different from anything the author has ever done before.

Special thanks go to Landsvirkjun for their funding of the project, and future research, through the Energy Research Fund.

This is dedicated to my son, Styrmir Logi Birgisson. I do this all for you.

Birgir Hrafn Hallgrímsson

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Introduction

Thermoelectric devices have two functions, either to convert electric current to temperature difference or to change temperature difference to electric current. This project will focus on the latter. The objective was to investigate the use of silicon as a material for constructing thermoelectric devices. Silicon is an inexpensive material and has interesting electrical and thermal properties which can be taylor made for various designs. It is also the most commonly used semiconductor material in electronics to date.

Thermoelectric generators (TEG) are devices to harvest energy from waste heat, see Fig. 1. The thermoelectric effect was discovered in 1821 by Thomas Johann Seebeck. TEGs have been studied ever since and by the 1950's generator efficiencies had reached 5% [9]. Today a waste heat conversion efficiency between ∼16.5% and ∼20% are predicted with a cold side temperature of 350 K and a hot side temperature of 650 K [10].

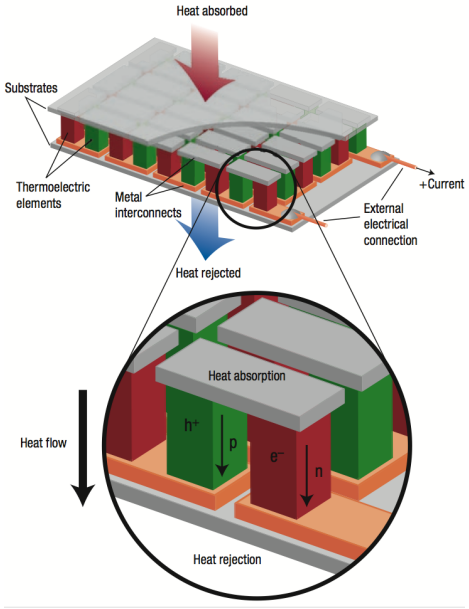

Figure 1: The basic structure of a TEG. Many thermocouples of n and p-type are connected in electrical series and thermal parallel [1]

There is an increased demand for environmentally friendly solutions in electric power production. Additionally there is a need for readily available power production to charge electronic devices used in places that would otherwise not have any capacity to offer electricity. A TEG is a possible answer to these needs.

The TEG has a clear advantage over other solutions, such as engines that need to carry their own fuel, when it comes to reliability and mobility. With no moving parts the solid state device can be used over several decades with no maintenance as in the Voyager missions of NASA [11].

TEG devices can be designed to take advantage of small temperature differences. They are easily scaleable for different power consumption cases, simple, inexpensive and

compact. Small generators can be mass-produced to recover energy from waste heat from internal combustion engines or from the run-off water from homes for example. The TEG has even been miniaturised to harvest energy from body heat to power a wristwatch [12]. The TEG can also be designed to work as a kind of solar cell, with a design on the hot surface side that would absorb the visible light spectrum and turn the light into heat. The same principle would apply as if the TEG were mounted to a waste heat supply, be it a wood burning stove or a pot of water heated by a primus gas stove.

TEG devices are commercially available from numerous companies, Sheetak, TEGPRO, Custom Thermoelectric and many others are offering both standard devices and custom designs for various applications.

The use of thermoelectric devices to recover electrical energy from sources of waste heat will grow in the future. As energy prices continue to rise the demand for more efficient solutions will continue to grow. There is an abundance of energy being wasted, both commercially and domestically, every day. With continued research into the nano-scale structure of semiconductors to be used as thermoelectric generators, the application fields will continue to grow.

A thin nanostructured TEG could prove effective in recovering wasted thermal energy in the form of electrical energy, reducing the load placed on generators and thus the diesel engine powering it. Industrial implementation is also applicable as all energy recovered from waste heat would reduce the electrical consumption from the supplier, reducing the load on carrier lines, transformers and generators. Smaller scale nanostructures are also feasible, where the heat from the human body would be used as a heat source and the environmental air temperature would provide cooling.

A suitable active material in thermoelectric devices should have high electrical conductivity and low thermal conductivity at the same time. Metals have high thermal conductivity and high electrical conductivity while insulators have low electrical conductivity and low thermal conductivity. Thus, a suitable material would be something with properties there between; a semiconductor. Being a semiconductor, silicon (Si) in its pure form has low electrical conductivity. By doping the silicon (intentional addition of foreign atoms), its conductivity can nevertheless be increased to an appropriate level. The thermal conductivity of silicon is however relatively high which makes bulk silicon impractical for thermoelectric applications. For an effective TEG device a temperature gradient is needed, the ideal material would be one which conducts electricity well but does not have any thermal conductivity.

Despite this, silicon was chosen in this project since recent studies have shown thermal conductivity in nanostructured silicon can be significantly reduced compared to that of bulk silicon. The aim of the present study is partly to gain fundamental knowledge and hands-on skills in processing a TEG. Thus providing a base for scheduled master study on nanostructured silicon TEG.

Chapter 1

Thermoelectric Devices

1.1 Semiconductors - Silicon characteristics

A semiconductor has, as the name implies, resistivity which is between that of an insulator, such as plastic, rubber and glass, and of a conductor, such as copper, silver or gold. Specific resistivity is quantified with the following equation

$$\rho = R \cdot \frac{A}{l} \ [\Omega\text{m}] \tag{1.1}$$

where R is the absolute resistance and A is the cross section area of a conductor of length l. The geometry can be seen in Fig. 1.1.

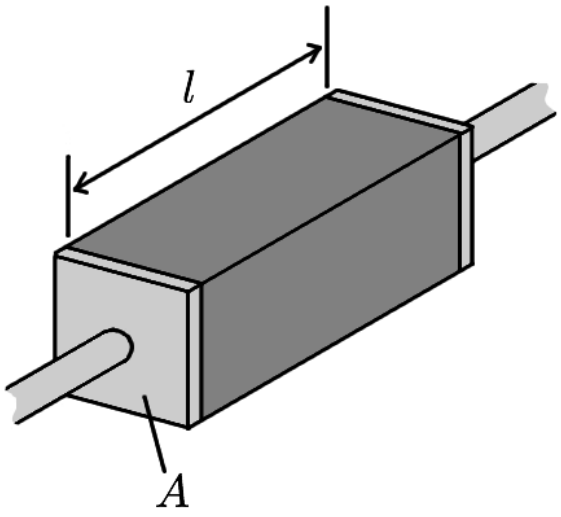

Figure 1.1: The geometry of a conductor with cross section A and of length l [2]

The specific resistivity ranging from conductor to insulator reaches from 10^{-8} Ωm (metal conductor) to 10^{16} Ωm and higher (insulator). The semiconductor will be in between these values as can be seen in Table 1.1.

The resistivity of semiconductors can be manipulated by up to 8 orders of magni-

Table 1.1: Specific resistivity of several materials [7]

Material	Specific resistivity (Ωm at 20°C)
Silver	$1.59 \cdot 10^{-8}$
Copper	$1.68 \cdot 10^{-8}$
Gold	$2.44 \cdot 10^{-8}$
Aluminium	$2.82 \cdot 10^{-8}$
Bismuth telluride	$9.1 \cdot 10^{-6}$
Germanium	$4.6 \cdot 10^{-1}$
Undoped silicon	$6.40 \cdot 10^{2}$
Glass	$1 \cdot 10^{10} - 10 \cdot 1^{14}$
Rubber	$1 \cdot 10^{13}$
Teflon	$1 \cdot 10^{22} - 1 \cdot 10^{24}$

tude [13] by adding impurities to its crystal lattice. The resistivity varies from 10^3 to 10^{-4} Ωcm for impurity concentration of 10^{12} to 10^{20} donor particles per cm^3 respectively. The electrical conductivity is caused by electrons and holes, which are released from donors and acceptors respectively (impurity doping atoms). Donor atoms have more valance electrons than the source material and acceptor atoms have fewer valance electrons than the source material. A selected portion of the periodic table where the best known semiconductor, Si, appears can be seen in Fig. 1.2.

Material	Thermal conductivity $[\frac{\mathrm{W}}{\mathrm{m\,K}}]$
Polyurethane	0.02-0.021
Paper	0.05
Polyethylene	0.42-0.51
Bismuth telluride	1.20
Marble	2.07-2.94
Stainless steel	18-24
Germanium	60.2
Silicon	149
Aluminium	250
Pure Copper	401

Table 1.2: Table of thermal conductivity of selected materials [8]

Only high purity silicon can be used as a semiconductor. The purity must reach nine nines, 99.9999999% (before impurity doping) pure silicon for so called electronic grade [14]. The resistivity of a silicon can be controlled by adding impurities. By adding impurities the number of charge carriers (holes and/or electrons) can be precisely controlled. Silicon is a period IV element, see Fig. 1.2. Atoms from period III (boron, gallium or indium) are acceptors and atoms from period V (phosphorus, arsenic or antimony) are donors. When p and n-type semiconductors have a conductive connection the holes from the p-type

swarm over to the n-type and the electrons from the n-type swarm over to the p-type.

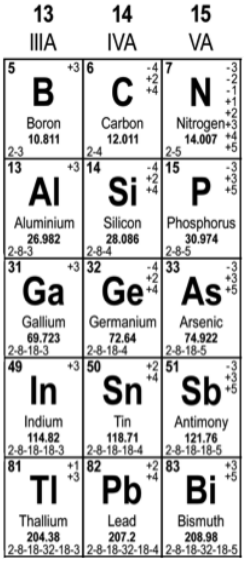

Figure 1.2: A selected portion of the periodic table where the best known semiconductors Silicon (Si) and Germanium (Ge) are found. Atoms from columns IIIA and VA can be used as acceptors and donors respectively

The elements in group IIIA to the left of Si have 3 valance electrons, and the elements in group VA to the right have 5 valance electrons. Since Si has 4 valance electrons, the impurity atoms will make an atomic bond with the silicon that has either a missing electron or an extra electron. The missing electron is referred to as a "hole" and leaves the bond positively charged, p-type conductivity. The extra electron is referred to as a negative charge, n-type conductivity. The electrons and holes can move through the crystal and thus carry an electric current. A schematic expression of this bond can be seen in Fig. 1.3.

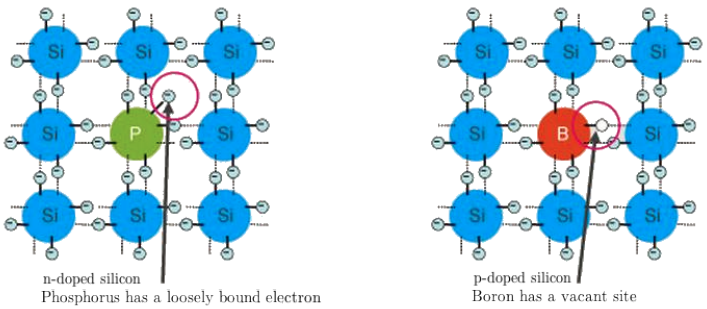

Figure 1.3: Graphical overview of n and p-type doping [3]

The energy levels of the electrons form bands of energy states, separated by an energy gap. The highest occupied band at zero temperature (0 K) is called the valance band and the first unoccupied band just above the energy gap is called the conduction band. Completely filled bands and completely empty bands cannot conduct electricity. In semi-

conductors, at any nonzero temperature, a small fraction of the electrons can overcome the energy gap [15].

The energy needed for an electron to cross the band gap in undoped silicon is 1.11 eV at 302 K [16] but in general the energy band gap of semiconductors tends to decrease as the temperature is increased. Impurity atoms create new energy levels in the energy gap. Donor atoms create levels relatively close to the conductive band and acceptor atoms create levels relatively close to the valance band. Thus only small energy is needed to promote the extra electrons to the conduction band. Similarly, the acceptor atom can easily capture electrons from the valance band atoms, leaving positively charged holes in the valance band. The holes leave behind them ionized acceptors (negatively charged) and the electrons ionized donors (positively charged) [17]. For thermoelectric uses the impurity concentration is typically between 10^{18} and 10^{20} atoms per cm^{-3} [1].

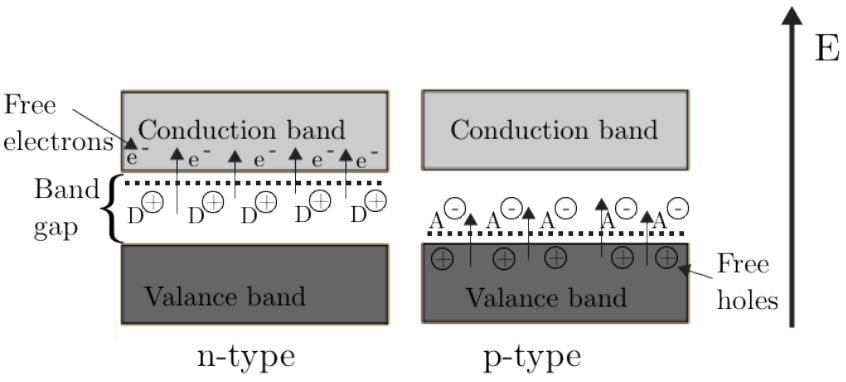

Figure 1.4: Energy band diagrams of n and p-type semiconductors where D denotes the donor and A the acceptor atoms

In Fig. 1.4 it is shown graphically that when one side of a TEC is heated the free electrons of the n- type material will move in an opposite direction to that of the free holes in the p- type. This is how the circuit will conduct electrical current when a temperature gradient is applied to the circuit.

Thermoelectric devices are conventionally made from semiconducting materials. Silicon is readily available in great abundance all over the world in the form of silicon oxides such as quartz. Because if its abundance it is a relatively inexpensive material compared to other options [18]. Silicon has relatively high thermal conduction, as can be seen in Table 1.2. It is therefore not an ideal bulk material for TEG devices since the distance from the hot side to the cold side will have to be considerably long in order to achieve a useful temperature gradient.

1.2 Thermal conduction in solids

The mechanism of thermal conductivity is mainly of two origins: **a)** Lattice vibration and **b)** Free electron diffusion as they diffuse through the crystal. Non metallic solids will only conduct heat through lattice vibrations and metals will conduct heat mainly via diffraction of free electrons.

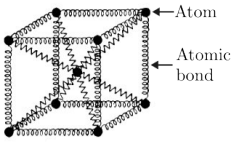

Figure 1.5: A simplified 3D model of a crystal lattice showing atoms and atomic bonds [4]

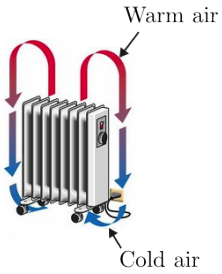

Figure 1.6: A simple figure showing air convection [5]

a) Lattice vibrations, also known as phonons, occur as vibrating atoms and molecules interact with neighbouring atoms and molecules transferring some of their thermal energy to them. The rate of heat transfer depends on the temperature gradient across the material and the thermal conductivity of the material. In a crystal the atoms are bound to one another in a repeating three-dimensional pattern. The bond between atoms can be described as a spring, shown schematically in Fig. 1.5. As the atom receives more energy it starts vibrating more violently, thus transferring some of its thermal energy to the neighbouring atoms through the atomic bond.

b) Electron diffusion can be compared to the thermal convection of molecules in gasses as "hot" electrons from higher energy states carry more thermal energy than "cold" electrons. Natural convection results from the tendency of most gasses to expand when heated. Circulation caused by this effect explains the uniform heating of air in a heated room. The heated molecules expand the space they move in through increased speed agains one another, rise, and the cool again and come closer together, with increased density and a resulting sinking as is shown in Fig. 1.6.

In a semiconductor, both forms of heat transfer occur as the material has both a crystal lattice and free electrons.

1.3 Seebeck Effect

Thermoelectric generators convert thermal energy to electric power. When heat is applied to one end of a semiconductor, heated charge carriers (either electrons or holes) flow toward the cooler end where there is a lower density of hot carriers (and vice versa). If a pair of n and p-type semiconductors are connected through an electric circuit, direct current (DC) flows through that circuit. This principle is called the Seebeck effect. The Seebeck effect is defined as the "production of an electromotive force (emf) and consequently an electric current in a loop of material consisting of at least two dissimilar conductors when two junctions are maintained at different temperatures" [19]. Conversely, a temperature difference is created when a voltage is applied to them. The voltages created by the Seebeck effect are small, usually in the order of a few μV per Kelvin of temperature difference across the semiconductor. Many such devices can be connected in series to increase the output voltage or in parallel to increase the maximum deliverable current. In this context, it can be mentioned that the Seebeck effect is responsible for the behaviour of the so-called thermocouples, which are commonly used as a thermometer.

The basic structure of a TEG can be seen in Fig. 1, where pairs of n and p-type semiconductors are connected in series to one another. These pairs, known as thermocouples, are then connected in series to build a higher voltage potential. A thermocouple, as can be seen in Fig. 1.7, works on the principle that when two conductors with dissimilar characteristics are connected will produce a voltage potential difference when heated.

The resulting potential voltage due to the temperature difference, ΔT, is proportional to the Seebeck coefficient α, as is given by the equation

$$V_{\mathrm{OC}} = \alpha \cdot \Delta T \tag{1.2}$$

where V_{OC} stands for the thermoelectric potential in an open circuit. A good thermoelectric couple will have a Seebeck coefficient between $\pm 100 - 300\ \frac{\mu \mathrm{V}}{\mathrm{K}}$ [12], so in order to produce a device that will have an electric potential in the order of a few mV or μV, many thermoelectric couples will need to be connected in series. The Seebeck coefficient of the materials used in this project will be measured and calculated using the formula

$$\alpha = \frac{V_{\mathrm{OC}}}{T_{\mathrm{H}} - T_{\mathrm{C}}} \tag{1.3}$$

where T_{H} is the temperature on the hot side and T_{C} is the temperature on the cold side.

The highest efficiency a heat cycle can possible have is defined by the Carnot cycle:

$$\eta_{\max} = 1 - \frac{T_{\mathrm{C}}}{T_{\mathrm{H}}} \tag{1.4}$$

It should be noted that today, this is still an unobtainable theoretical maximum efficiency.

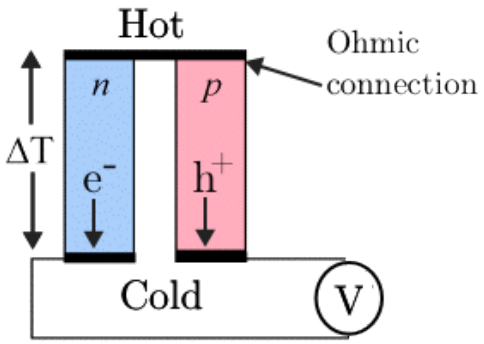

Figure 1.7: Schematic of a thermocouple circuit

The maximum efficiency of a TEG using the Seebeck effect is given by

$$\eta_{\max} = \frac{T_{\mathrm{H}} - T_C}{T_{\mathrm{H}}} \frac{\sqrt{1 + Z\bar{T}} - 1}{\sqrt{1 + Z\bar{T}} + \frac{T_{\mathrm{C}}}{T_{\mathrm{H}}}} \tag{1.5}$$

where $Z\bar{T}$ denotes the modified figure of merit where the thermoelectric capacities of the materials used to form a thermocouple in the TEG are taken into consideration. $Z\bar{T}$ is given by

$$Z\bar{T} = \frac{(\alpha_{\mathrm{p}} - \alpha_{\mathrm{n}})^2 \bar{T}}{[(\rho_{\mathrm{n}}\kappa_{\mathrm{n}})^{1/2} + (\rho_{\mathrm{p}}\kappa_{\mathrm{p}})^{1/2}]^2} \tag{1.6}$$

where ρ denotes the electrical resistivity, $\bar{T}$ the average temperature of the hot and cold ends and κ the thermal conductivity. The α_{n} and α_{p} denote the Seebeck coefficients for the n and p-type materials used in the thermocouple respectively. Since the same type of material (Si) is being used for both types, this formula can be somewhat simplified to the form of

$$ZT = \frac{\alpha^2 \sigma T}{\kappa} \tag{1.7}$$

From Eq. (1.7) it can be deducted that the optimal thermoelectric device would have a high Seebeck coefficient, α, high electrical conductivity, σ and low thermal conductivity, κ. A drawback to using silicon as a thermoelectric material is its low figure of ZT value, which is due to the high κ value at room temperature. For this reason, silicon has not been considered as a thermoelectric material and most of todays production uses bismuth telluride, with a ZT of 0.9 which had been the upper limit for more than 40 years. However, for instance silicon nanowires (SiNWs) have become an attractive option, since its nanostructure decreases the κ value. A method has been proposed to raise the ZT value higher than 1 using nanostructured silicon [20]. By successfully using nanostructuring to reduce the κ value, figures of merit as high as 1.5 - 1.9 have been achieved at temperatures ranging from 750 - 900 Kelvin [21]. Claims of even higher ZT values have been published as the long desired ZT value threshold of 2 has been reached [10]. There is no theoretical

upper limit for the ZT value, so as research progresses in the nanoscale structures there should be an ever increasing ZT value available.

A numerical comparison of Eq. (1.4) and (1.5) at 350 K and 650 K for the cold and hot side respectively and a ZT value of 2.2 give us a Carnot efficiency of 46.2% while the efficiency for the thermoelectric generator is 15.6%.

Chapter 2

Experiments

To make a wafer ready to be used in a TEG there are several steps which are necessary in order to achieve the needed attributes.

- The native oxide layer must be removed
- The wafer must be covered with a conducting metal
- An ohmic contact must be created
- The wafer must be diced into smaller pieces
- Each n and p- pair must have an electrical connection
- All the TEC pairs must be connected to each other
- Heat sinks must enclose the TEG with a hot side and a cold side

In the beginning of the project, phosphorus doped (n-type) and boron doped (p-type) Si wafers, 100 mm in diameter, from University Wafers were used. The n-type wafers were doped with phosphorus with resistivity of $6 - 14$ Ωcm and the p-type wafers were doped with boron with resistivity of $16 - 24$ Ωcm. These values correspond to impurity concentration on the order of 10^{15} cm^{-3}. These were later found to be unusable and were replaced with a 76 mm n-type wafer with resistivity < 0.009 Ωcm and a 100 mm p-type wafer with $0.01 - 0.02$ Ωcm resistivity. This corresponds to impurity concentration on the order of 10^{18} cm^{-3}

In this section I will explain the steps taken and the measurements made in order to make a functional thermoelectric device.

2.1 Instrumentation - Silicon thermoelectric device

2.1.1 Removing the native oxide layer

In atmosphere, silicon will react with oxygen and form a layer of native oxide (SiO_2) creating an insulating film. The thickness of this layer is a finite value in the range of 10-15 Å. Measurements were made to confirm this, where the native oxide layer was found to be just under 1.5 nm (15 Å). The measurements were made with the X-ray equipment PANalytical's X'pert diffractometer.

There are two methods which are mainly used to remove the SiO_2 layer. Either by using Rapid Ionic Etching (RIE) or by using Hydrofluoric acid (HF acid). The RIE process is referred to as a "dry etching process" and the acid process as "wet etching". The wet etch was chosen for this project for a few reasons; It is an easy process and an inexpensive one. However, one must be very careful when working with HF acid since it is highly corrosive and skin exposure to as little as 160 cm^2 can be fatal [22].

A solution of HF acid and de-ionized water was made with 9 parts water and 1 part HF acid, 10:1 HF. The acid had a concentration level of 40% and the etch time was always over 2 minutes at room temperature [23]. A special wafer holder of teflon was made for this project, so that the silicon wafer would not stick to the bottom of the solution cup, as shown in Fig. 2.1

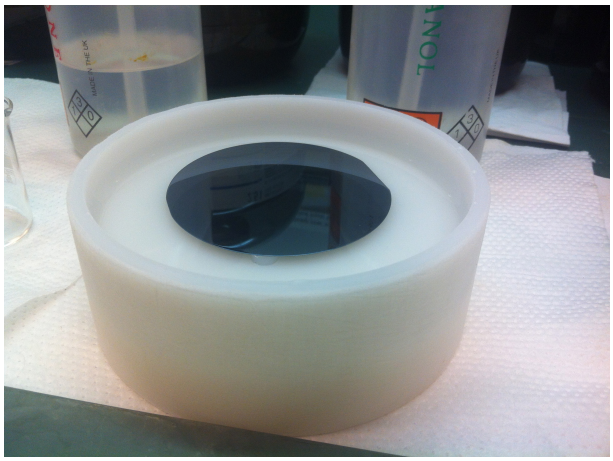

Figure 2.1: A 76 mm silicon wafer in a wet etching process

The HF acid solution was rinsed from the substrate using de-ionized water first and isopropanol afterwards. To reduce contact with oxygen on the freshly etched silicon surface the silicon wafer was placed in a cup of de-ionized water for transportation to the metal deposition. This should reduce the formation of SiO_2 on the substrate. Measurements would confirm that the SiO_2 layer that formed while waiting for metal deposition was negligible, 1-3 Å thick.

2.1.2 Metal deposition

When n and p-type semiconductors come in contact with each other, they will conduct electric current from the p-type (anode) to the n-type (cathode) and block the current from going in the other direction, such kind of p-n junctions are called Schottky diodes. A schematic of such rectifying behaviour can be seen in Fig. 2.2 a). For a functional device, the conductivity of the n and p-type thermocouples must be ohmic, that is; a linear current vs. voltage behaviour as can be seen in Fig. 2.2 b).

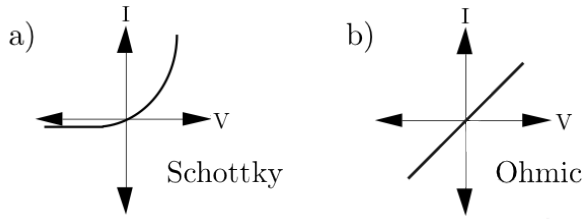

Figure 2.2: IV curves showing Schottky and ohmic conductivity

To make an ohmic contact on the silicon a thin layer of aluminium (Al) was deposited on the silicon wafer. For the deposition process a Cryofox Explorer 600 was used, see Fig. 2.3. An electron beam (e-beam) melts a source metal (Al), which evaporates and deposits onto the Si-substrate in the vacuum chamber. The deposition is carefully monitored and the deposition rate can be adjusted to suit the needs of the user.

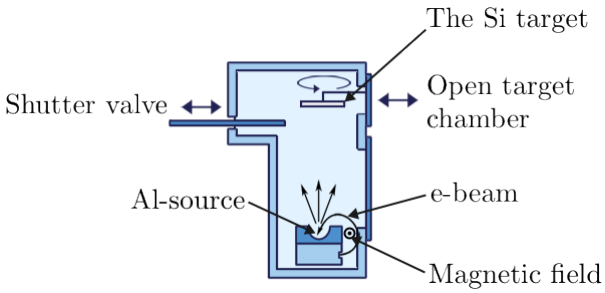

Figure 2.3: A schematic of the e-beam evaporation process [6]

The silicon wafer is placed on a special holder which goes into the process vacuum chamber. A flat surface, as seen in Fig. 2.4, can be used for wafers up to 100 mm in diameter and using special adhesive tape which does not emit gasses when under vacuum. There is also a special holder for 100 mm wafers which is basically an open rim and can hold the wafer without the need to use any tape.

The process parameters were a deposition rate 10 of Å/s and a total thickness of 200 nm at an air pressure of $6 \cdot 10^{-6}$ mbar.

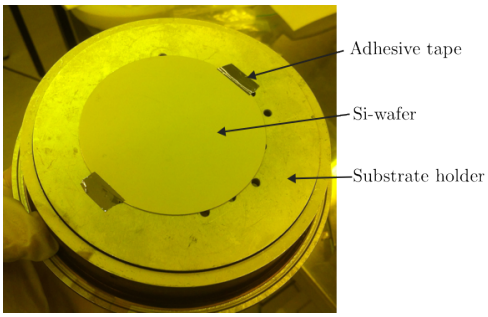

Figure 2.4: A 76 mm silicon wafer after metal deposition

2.1.3 Cutting the wafers

To divide the silicon wafers down to preferred sized there were two methods available, using a diamond scribe pen to cut along the surface of the wafer and then crack the wafer by hand. This would often result in unwanted shapes of the dices and meant that the wafer needed to be cut before the metal deposition. The other option was to use the Loadpoint Microace 3, which is a semiautomatic, programmable and extremely precise cutting machine. The latter option was chosen for this project.

The dicing saw used is a Loadpoint Microace 3, which is a semiautomatic saw for wafers up to 100 mm in size. The blades can be both hubbed and hubless, the hub blades being 20 μm in thickness while the hubless blades range from 150 to 200 μm. The saw can cut through silicon, glass and quartz wafers up to 3 mm thick.

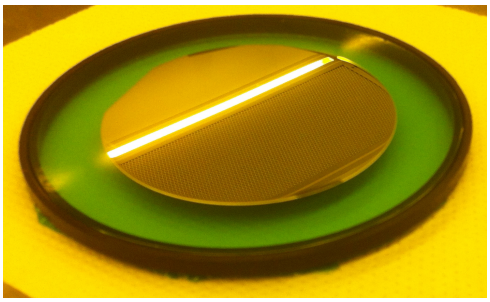

Figure 2.5: A 76 mm silicon wafer placed on an adhesive film

The dicing saw has very high resolution and can be set to dice wafers down to micro scale. For this project many different size dices were tested, but in the end a 10×10 mm size was chosen.

By cutting the entire wafer into the same size dices the waste of material is minimised.

2.1.4 Rapid thermal annealing

To reduce the contact resistivity of the Al-Si junction(i.e. create ohmic contact), rapid thermal annealing (RTA) methods were utilised. This was also thought to be a necessary step to avoid Schottky behavior at the junction of the aluminium and the n-type silicon,

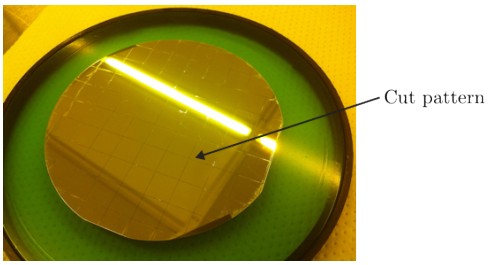

Figure 2.6: A 100 mm wafer diced into 10×10 mm^2 squares

since aluminium may behave as an acceptor to silicon. To create an ohmic contact the metal must transport into the silicon, connecting the electrons and holes to the metal surface.

The RTA machine available in the clean lab is the Jipelec Jetfirst processor. It can provide a vacuum and inject gasses into the processing chamber before annealing to avoid oxidising the aluminium.

On the first batch of wafers many different recipes were tried, with the temperature ranging from 300-1000°C. After many attempts and IV curve measurements nothing seemed to work properly. A recipe of a 425°C for a few seconds was said to give the best results [24]. To prevent oxidation on the aluminium film the process chamber is first vacuumed and then injected with nitrogen (N_2) gas before annealing.

As will be explained in section 2.1.4, measurements indicated that the best conductivity of the metal deposited silicon dices was by not annealing them at all, hence this method was not used after this discovery.

2.1.5 IV measurements

To determine the best results from the metal deposition and RTA process IV measurements had to be made. In this process DC voltage was applied in steps from a voltage source to a sample of silicon, in a manner shown schematically in Fig. 2.7.

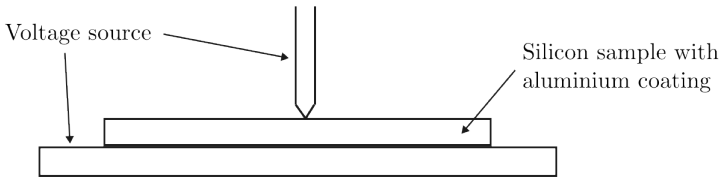

Figure 2.7: The IV mesurement setup

For every voltage step, the current was measured. With this data an IV curve can be drawn for each sample. Different sized silicon samples were measure, 2×2 mm^2, 4×4 mm^2, 6×6 mm^2, 8×8 mm^2 and 10×10 mm^2. The measurements were made using four-terminal sensing to increase accuracy in the readings.

The first silicon samples to be tested had a resistivity range of $16 - 24$ Ωcm for the p-type and $6 - 14$ Ωcm for the n-type.

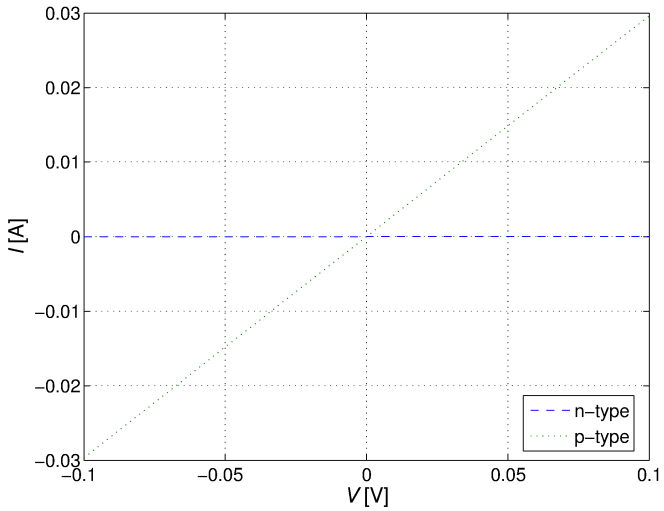

Figure 2.8: The IV curves of typical n and p-type samples

As can be seen in Fig. 2.8 the difference in conductance for the n and p-type samples is considerable. Looking closer at the n-type sample in Fig. 2.9 it is obvious that there is an ohmic contact. However, with the resistance of the sample in the order of $10^3\Omega$ (and even higher in other samples using different RTA methods) the current was in the μA scale, which is unacceptably low. For the p-type sample there were less problems, but a resistance in the order of 1 Ω is also unacceptable.

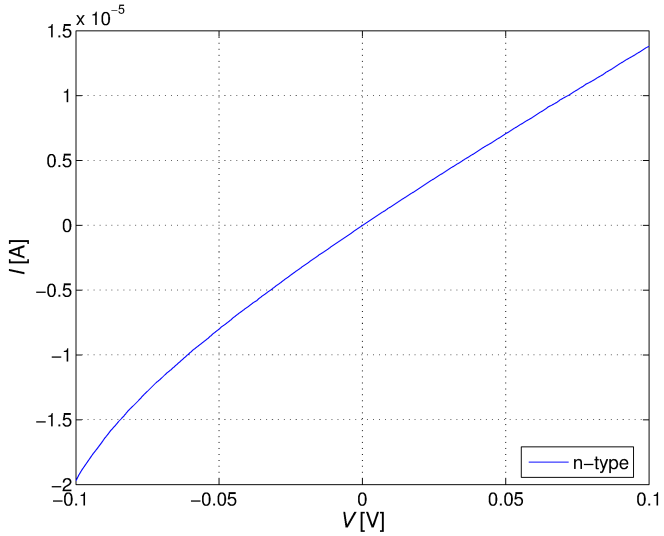

Figure 2.9: The IV curve of a typical n-type sample

The new wafers with higher impurity concentration were then treated and tested. Again, trying different RTA recipes both the n and p-type samples showed high resistance and unwanted behaviour. By not annealing the samples at all, they would have very similar resistance and ohmic behaviour as can be seen in Fig. 2.10

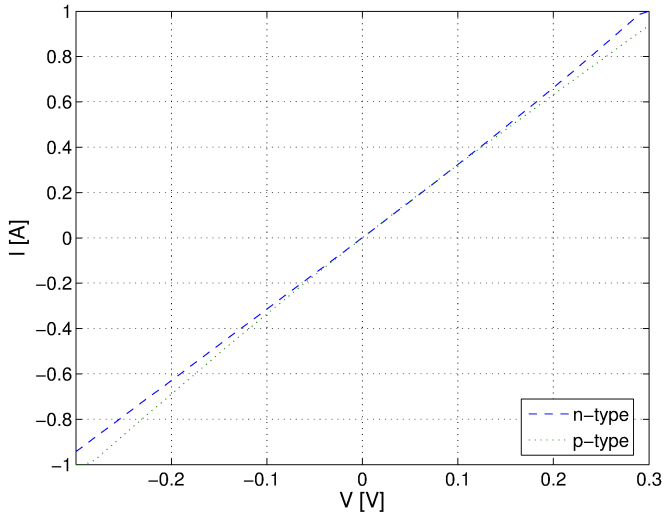

Figure 2.10: The IV curve of the new n and p-type samples

With resistances in the order of $10^{-1}\Omega$ an optimal size for the silicon sample was found. 10×10 mm with no RTA treatment. The sample thickness varied, as the n-type was 0.420 mm thick and the p-type 0.525 mm thick.

2.2 Device construction

To construct a device, two extra components are needed. An electrical conductor to connect each n and p-type TEC pair as well as form the series connection from one TEC to another. Substrates will have to enclose the electric circuit which will need to have good thermal conduction and no electric conductance. The structure is shown schematically in Fig. 1.

Two different alignments were tested. The silicon dices were aligned flat (horizontal), Fig. 2.11 and standing up on the thin side of the material (vertical), Fig. 2.12. The vertical alignment should give a better temperature gradient and result in higher Seebeck voltage and a better Seebeck coefficient.

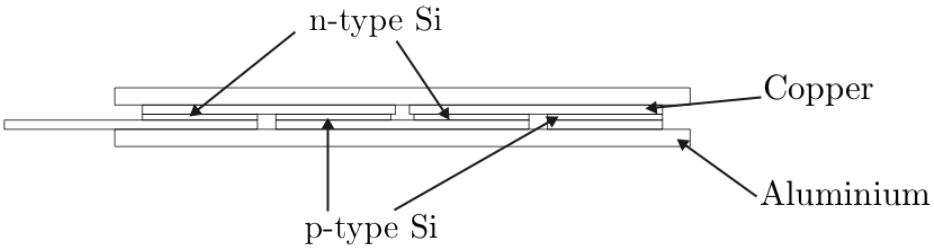

Figure 2.11: A side view of the horizontal arrangement of the Si dices

For electrical conduction copper plates 10×22 mm^2, 0.8 mm thick were used as an electrical conductor between the n and p-type semiconductors. The hot and cold side substrates are made of anodized aluminium 1.5 mm thick. Anodizing is a special treatment used to increase the native oxide layer on aluminium. Its name is derived from the process, where the aluminium to be anodized forms the anode electrode of an electrical circuit. The native oxide layer thickness on aluminium is from 2 to 3 nm thick [25] which can be increased to 0.5 to 150 μm with the anodizing process. The thin layer of aluminium oxide (Al_2O_3) provides the electrical insulation and the aluminium gives great thermal conduction.

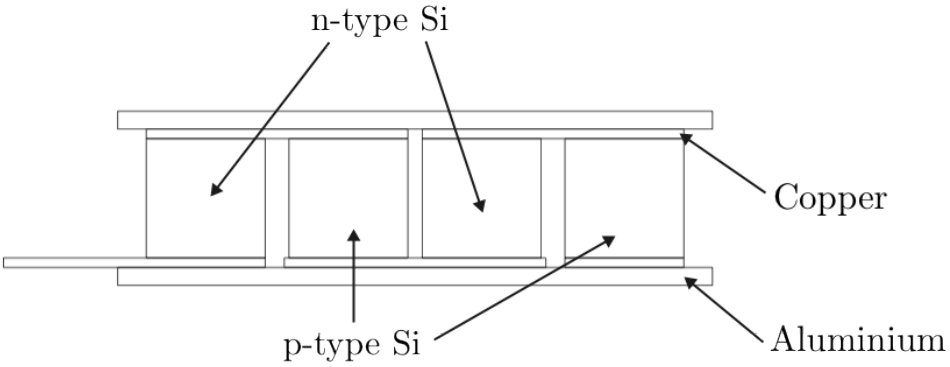

Figure 2.12: A side view of the vertical arrangement of the Si dices

The copper plates were attached to the aluminium substrates using Epoxy Universal from Bison [26] and to bond the n and p-type silicon dices to the copper plates H20E silver adhesive from Epoxy Technology [27] was used. The silver adhesive was chosen for its good electrical properties with volume resistance at 23°C $\leq$ 0.0004 Ωcm.

Three different devices were made. Two with horizontal alignment of the Si dices and one with vertical alignment (devices 1,2 and 3 respectively). On the horizontal arrangement the ohmic contacts were made on the surface of the silicon dices and on the vertical alignment the ohmic contact was made on the lateral part.

To assemble the devices with horizontal arrangement the copper plates were glued to the aluminium substrates and pressure applied for 1.5 hours while the Epoxy set. Silver adhesive was then applied to the copper plates and the TEC pairs assembled, the piece placed on a hot plate at around 150°C and pressure applied for about 10 minutes while the adhesive dried. Silver adhesive was then applied to the top of the silicon dices and copper placed on top of them to complete the electric circuit, again heat baked and pressure applied. Finally epoxy was applied to the copper plates on top and an aluminium substrate placed on top to complete the device.

Device 1

Device 1, shown in Fig. 2.13, was made with one TEC pair in a horizontal arrangement.

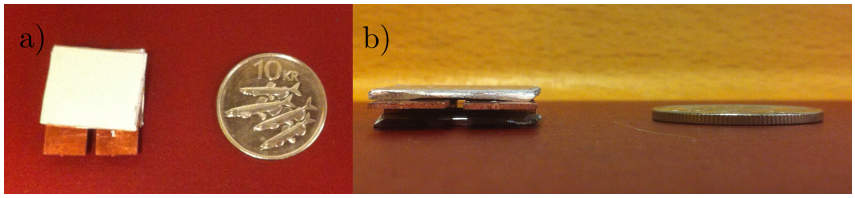

Figure 2.13: a) Top view of device 1 b) Side view of device 1. Horizontal arrangement

Device 2

Device 2, shown in Fig. 2.14, was made with 8 TEC pairs in a horizontal arrangement.

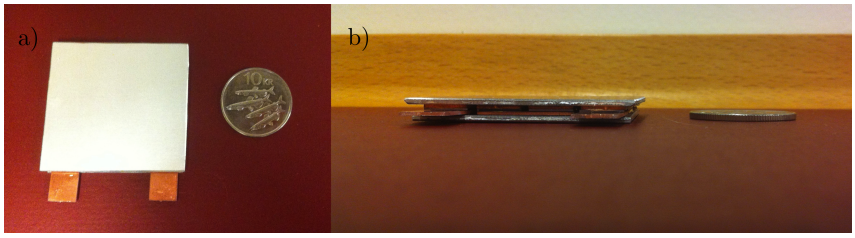

Figure 2.14: a) Top view of device 2 b) Side view of device 2. Horizontal arrangement

Device 3

Device 3, shown in Fig. 2.15, was made with 8 TEC pairs in a horizontal arrangement.

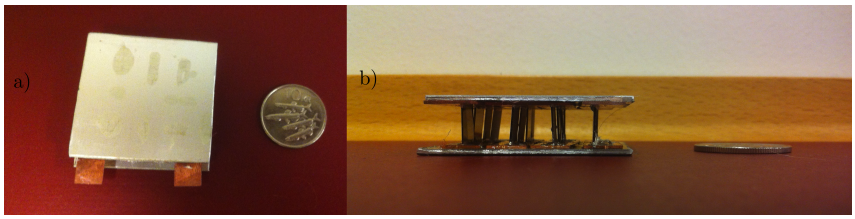

Figure 2.15: a) Top view of device 3 b) Side view of device 3. Vertical arrangement

For device 3 a template had to be made to keep the silicon dices on a vertical position. The template was made from cardboard and the silicon arrangement cut into it with a knife. To keep the pieces in a perfect vertical position proved impossible so the silicon dices are sometimes awry. Due to both the assembly time and the heat applied to cure the silver adhesive, a significant layer of SiO_2 was able to form which has a very negative electrical effect.

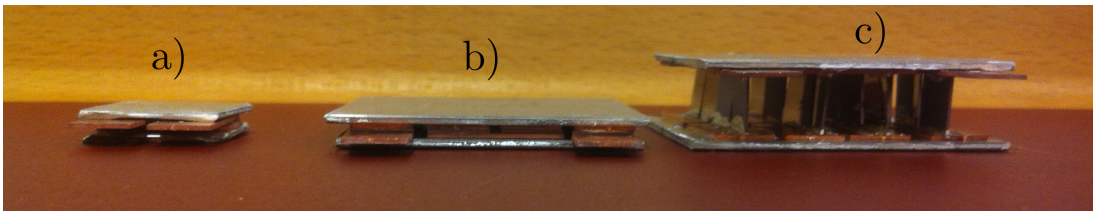

Figure 2.16: a) Device 1 b) Device 2 c) Device 3

As seen in Fig. 2.16 there is a significant difference in the thickness of devices 1 and 2 compared to 3.

2.3 Device performance

To find the Seebeck coefficient α as described in Eq. (1.3) a measurement experiment was set up. A glass container was attached to the cold side of the TEG device and thermal conductivity with the aluminium substrate was improved by using thermal conductive paste (thermal grease) as is used to conduct heat from a processor to a heat sink for example. Ice cubes were set in the glass container and the mix of water and ice gives a reference temperature of 0°C. The hot side of the TEG device was not connected to a heat source and was thus at room temperature. The temperature on the hot side was measured with a FLUKE 289 multimeter, whose temperature range is -200°C - 1350°C with a basic accuracy of ±1.0% [28].

The thermocouple of the FLUKE was attached to the hot side substrate of the TEG and voltage readings were made at the same time as the temperature was read. The temperature on the hot side dropped as the materials conducted heat and a drop in voltage was observed as can be seen in Fig. 2.19.

Voltage and current measurements were also made where the devices were placed on a hot plate which was heated up to 200°C and ice cubes were placed on the cold side as before.

Device 1

With 2 individual pieces (1 TEC pair) the device had a Seebeck coefficient of $-3.84\ \frac{\mu V}{K}$, as seen in Fig. 2.17. The individual piece Seebeck coefficient for the material is this $-1.92\ \frac{\mu V}{K}$. The resistance of the device was measured 1.01 Ω.

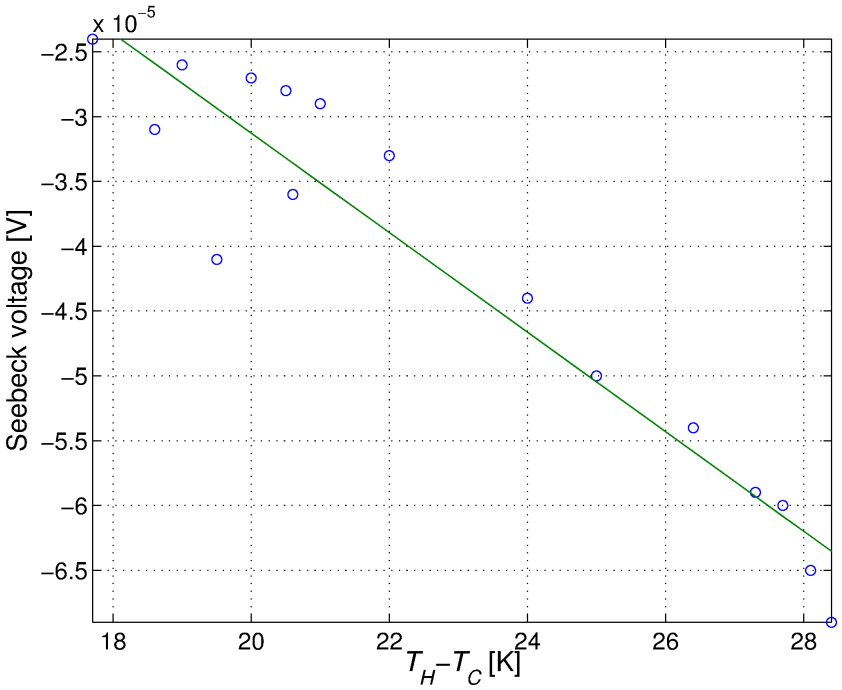

Figure 2.17: The Seebeck voltage as a function of a temperature gradient

The device produced -1 mV_{DC} and -12 μA_{DC} on the hot plate test which equals to $-5\ \frac{\mu V}{K}$.

Device 2

With 2 individual pieces (1 TEC pair) the device had a Seebeck coefficient of $-16.9\ \frac{\mu V}{K}$, as seen in Fig. 2.18. Each TEC then has a Seebeck coefficient of $-2.11\ \frac{\mu V}{K}$. The individual piece Seebeck coefficient for the material is this $-1.05\ \frac{\mu V}{K}$. The resistance of the device was measured 310 Ω.

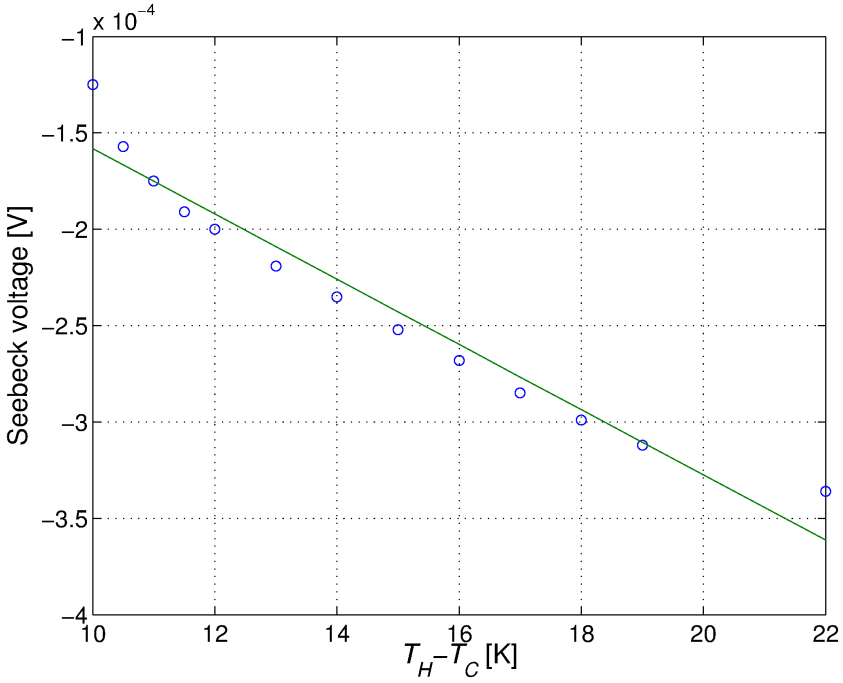

Figure 2.18: The Seebeck voltage as a function of a temperature gradient

The device produced -5.4 mV_{DC} and -21 μA_{DC} on the hot plate test which equals to $-3.37\ \frac{\mu V}{K}$.

Device 3

With 16 individual pieces (8 TEC pairs) the device had a Seebeck coefficient of $-1.74\ \frac{\mathrm{mV}}{\mathrm{K}}$, as seen in Fig. 2.19. Each TEC had a Seebeck coefficient of $-217\ \frac{\mu\mathrm{V}}{\mathrm{K}}$. The Seebeck coefficient for each piece is $-108.9\ \frac{\mu\mathrm{V}}{\mathrm{K}}$. With measured resistance close to $\approx 2\ \mathrm{M}\Omega$, the current produced by the device is negligible and thus its efficiency will be $<< 1\%$. This high resistance may be attributed to both contact resistance and the oxide layer that was able to form as the silicon was exposed to air.

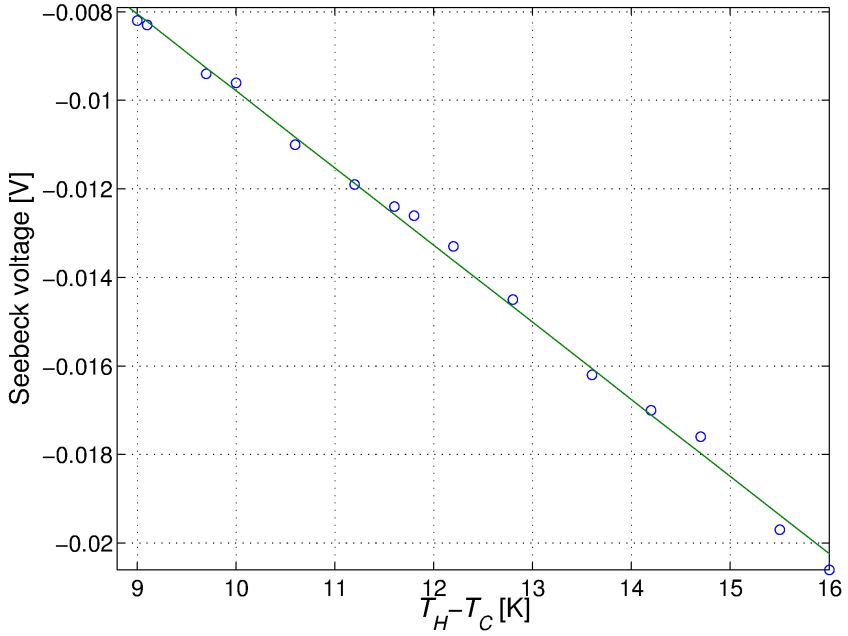

Figure 2.19: The Seebeck voltage as a function of a temperature gradient

The device produced up to -80 $\mathrm{mV_{DC}}$ but it had no measurable current on the hot plate test which equals to $-50\ \frac{\mu\mathrm{V}}{\mathrm{K}}$.

Measurement data

Table 2.1: Measurement data table for device 1

T_H [K]	T_C [K]	$T_H - T_C$ [K]	Voltage [mV]
298.15	273.15	25	-0.050
297.15	273.15	24	-0.044
295.15	273.15	22	-0.033
294.15	273.15	21	-0.029
293.65	273.15	20.5	-0.028
293.15	273.15	20	-0.027
292.15	273.15	19	-0.026
290.85	273.15	17.7	-0.024
291.75	273.15	18.6	-0.031
292.65	273.15	19.5	-0.041
300.45	273.15	27.3	-0.059
300.85	273.15	27.7	-0.060
301.25	273.15	28.1	-0.065
301.55	273.15	28.4	-0.069
299.55	273.15	26.4	-0.054
293.75	273.15	20.6	-0.036

Table 2.2: Measurement data table for device 2

T_H [K]	T_C [K]	$T_H - T_C$ [K]	Voltage [mV]
295.15	273.15	22	-0.336
292.15	273.15	19	-0.312
291.15	273.15	18	-0.299
290.15	273.15	17	-0.285
289.15	273.15	16	-0.268
288.15	273.15	15	-0.252
287.15	273.15	14	-0.235
286.15	273.15	13	-0.219
285.15	273.15	12	-0.200
284.65	273.15	11.5	-0.191
284.15	273.15	11	-0.175
283.65	273.15	10.5	-0.157
283.15	273.15	10	-0.125

Table 2.3: Measurement data table for device 3

T_H [K]	T_C [K]	$T_H - T_C$ [K]	Voltage [V]
289.15	273.15	16	-0.0206
288.65	273.15	15.5	-0.0197
287.85	273.15	14.7	-0.0176
287.35	273.15	14.2	-0.0170
286.75	273.15	13.6	-0.0162
285.95	273.15	12.8	-0.0145
285.35	273.15	12.2	-0.0133
284.95	273.15	11.8	-0.0126
284.75	273.15	11.6	-0.0124
284.35	273.15	11.2	-0.0119
283.75	273.15	10.6	-0.0110
283.15	273.15	10	-0.0096
282.85	273.15	9.7	-0.0094
282.25	273.15	9.1	-0.0083
282.15	273.15	9	-0.0082
281.95	273.15	8.8	-0.0079

Chapter 3

Discussion and conclusions

The results clearly indicate that Device 3 showed the best performance with a Seebeck coefficient of $-217\ \frac{\mu V}{K}$ at its best. However a more conservative result is that of $-50\ \frac{\mu V}{K}$ on the hot plate test. A good TEC pair will have a Seebeck coefficient in the range of $\pm(100-300)$; $\frac{\mu V}{K}$ [12]. The author suspects a lateralization error in the voltage measurements when the higher Seebeck coefficient value was obtained, since the curve is linear as was to be expected. The voltage, and thus the Seebeck coefficient realistically, should be lower.

The silicon wafers used in this project were very thin, 0.420 - 0.520 mm thick. A temperature gradient over such thin material is always going to be very small (in horizontal arrangement), if not negligible. Thus, having made a device that gave measurable voltage and current with these thin wafers is a small achievement in itself.

The difference in the active region for the TEG devices is a huge factor. With the silicon dice thickness around 0.5 mm there is virtually no temperature gradient, however placing the dices in a vertical arrangement device 3 has the highest temperature gradient, so it was expected that the Seebeck coefficient for the device would be the highest. With no measurable current due to the extremely high internal resistance, device 3 can be said to have practically zero efficiency. Its orientation will also make it extremely fragile, as the thin silicon wafers are a very brittle material, any lateral load of significance could very well break the device.

With Seebeck coefficients for devices 1 and 2 well below what is considered useful, the efficiency of these devices will always be negligible. There is also a notable difference in the resistance of devices 1 and 2. With 8 pairs in device 2 one would expect to see a device resistance of around 8 Ω. However the wafers are not of the same thickness and the thinner silicon pieces might not have a perfect contact to the electrically conducting copper as the silicon was pressed down with a flat substrate while the silver adhesive was drying and forming a bond.

Construction factors on device 3 will have an effect, such as the forming of a native oxide layer while waiting for assembly, contact and contact resistance. With these factors, piecing together a high efficiency TEG device would prove very hard, if not impossible. To

use silicon as a bulk material for a TEG construction, one would need a thick and highly doped wafer (2 mm or more) which would then be treated to oxide removal and metal deposition. A thicker material would also probably need RTA treatment for the deposited aluminium to swarm into the silicon. Such devices would however always prove inferior to devices already available made from bulk materials, in particular bismuth telluride.

Chapter 4

Summary

Three devices were constructed with two devices having a horizontal alignment of the silicon dices used having an active region thickness of 0.5 mm. One device was made with a vertical alignment with an active region thickness of 10 mm.

With a vertical orientation of the silicon pieces, device 3 had the highest Seebeck coefficient of $-217\ \frac{\mu V}{K}$ per thermocouple pair while devices 1 and 2 had a Seebeck coefficient of $-3.84\ \frac{\mu V}{K}$ and $-2.11\ \frac{\mu V}{K}$ respectively.

Testing the TEG devices on a 200°C hot plate with ice cubes in a tray on top of the devices yielded in -1 mV_{DC} and -12 μA_{DC} for device 1, -5.4 mV_{DC} and -21 μA_{DC} for device 2 and -80 mV_{DC} and 0.0 μA_{DC} for device 3. These measurements result in Seebeck coefficients of $-5\ \frac{\mu V}{K}$, $-3.37\ \frac{\mu V}{K}$ and $-50\ \frac{\mu V}{K}$ for devices 1, 2 and 3 respectively. Resistance was measured 1.01 and 310 Ω for devices 1 and 2 respectively and over 2 MΩ for devices 3.

As expected, it was observed that unmodified silicon wafers are not very suitable for being used as a thermoelectric generator.

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