Density of interface states at insulator/SiC interfaces.

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DENSITY OF INTERFACE STATES AT INSULATOR/SIC INTERFACES.

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16 ECTS thesis submitted in partial fulfillment of a
Baccalaureus Scientiarum degree in Physics

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To Alla for her unwavering support, to my father for his inspiration and to Ragnhildur for being an being an all-around kick in the butt.

Abstract

The need for an alternative to the prevailing Si based semiconductor devices is ever present, since the Si devices are fast approaching their limits. Some effort has gone into the study of SiC based devices in the past 20 years or so as an alternative for high power applications. However the SiC/SiO_2 interface has presented a number of challenges, due to the large number of interface traps. In this project we characterized these traps using three different capacitance-voltage measurement techniques on four different MOS - Capacitors, and found that most of these traps are present near the interface itself. One of the devices we looked at had been oxidized using a sodium enhanced oxidation process, which neutralizes most of the interfacial traps.

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1 Density of interface states at insulator/SiC interfaces.

1.1 SiC and its potential in semiconductor devices

Silicon (Si) is by far the most widely used semiconductor in the world today, but the dependance of the semiconductor industry on Si has begun to be problematic since Si-based devices are reaching their theoretical and material limits. One of the more promising alternatives is silicone-carbide (SiC). SiC is composed of tetrahedral of carbon and silicon atoms with a tightly bound crystal lattice. This leads to an extremely stable crystal structure and a near infinite number of polytypes. Some of these polytypes have manifested a number of characteristic which outperform traditional Si semiconductors:

- **Higher critical electric field**, ~ 8 times higher than that found in Si.
- **Higher thermal conductivity**, ~ 3.3 times higher than that found in Si.
- **Higher operating temperature**, $\gtrsim 770$ K compared to $\lesssim 420$ K for Si based devices.
- **Higher Current density**, $\sim 2-3$ times that of Si.
- **Wider bandgap**, (2.0 eV $\lesssim E_g \lesssim$ 3.6 eV for 4H-SiC and 6H-SiC or around 3 times times that of Si.

These characteristics make SiC an excellent choice for high power, high efficiency and even harsh environment power device applications. (1) (2) (3).

1.2 Oxidation of SiC and associated problems

The extremely stable structure of SiC results in the fact that it does not react with any known chemicals up to 800°C, however when heated up to 950°C it starts to react with oxygen and forms a thin layer of Silicon Oxide at its surface. This is a useful characteristic which is utilized with in the fabrication of SiC-MOS devices. SiC 4H-MOSFET devices have thus far been hampered by unacceptably low electron inversion channel mobilities typically in the range of 5-40 $cm^2/V \cdot s$. The low mobility is attributed to high density of interface states near the SiC conduction band edge resulting in charge trapping and Coulomb scattering at the interface.
When trying to explain the properties of the SiC/SiO_2 boundary there are certain advantages in comparing it to the well-known Si/SiO_2 boundary (4).
A key difference between the oxidations of Si and SiC, both of which produce SiO_2, is that in the SiC case large amounts of carbon atoms are released. It is generally believed that most of the C atoms are released as either CO or CO_2 through the growing oxide. The residual carbon at the SiC/SiO_2 boundary has been is believed to be the primary origin of the high density of interfacial defects (D_{IT}) and subsequently the hampered electron inversion channel mobilities (5). This has resulted in the realization of two major differences between the interface states of the two. First there does not seem to be an effective way of neutralizing the interface traps in SiC/SiO_2 boundary with hydrogen as is done in silicon devices. Secondly the electrical behavior of the traps differs somewhat from dangling bonds centers at the (111) Si/SiO_2 boundary.
The energy distribution and stability of the interface traps at the SiC/SiO_2 boundary has led researchers to believe that these traps can be explained by thermally released carbon from the SiC structure, the validity of this assumption was later enhanced by direct observation. Other sources of interface traps have been suggested such as the existence of a H-complexed oxygen vacancy acting as an electron trap and other inherent oxygen defects (5). These traps result in severe degradation of the surface electron mobility in SiC- MOS devices for certain polytypes which is attributed to the high density of interface traps created by the afore mentioned processes. The highest density of such traps is found at the 4H-SiC/SiO_2 interface. These are believed to be "near-interface traps" and are ascribed to distinct intrinsic defects in the interfacial region of the thermally grown SiO_2 (2). One of the tested samples was grown by a sodium enhanced reaction and it has been demonstrated to result in a strong reduction in the density of near interface traps at the SiC/SiO_2 interface (11).

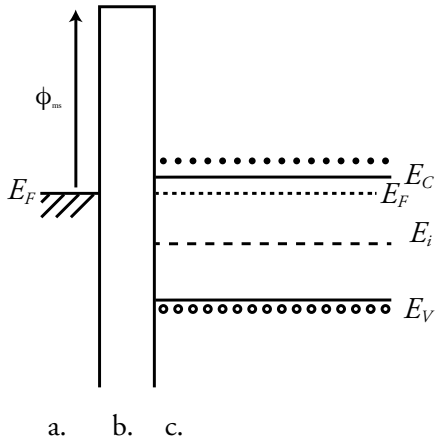

Figure 1.1: Energy band diagrams for a n-type MOS device at $V = 0$. ϕ_{ms} is the work-function of the metal, E_F is the semiconductor Fermi level, E_C the conduction-band energy level, E_V the valence energy level and E_i is the intrinsic energy level of the semiconductor. Electrons are represented by filled circles and holes by outlined circles. ***a.*** *is the metal gate,* ***b.*** *the oxide and* ***c.*** *is the semiconductor.*

1.2.1 CV and interface trap characterization

To get a sense of the effects of interface traps at the SiO_2/SiC interface one needs to consider the energy band diagram of the device, fig. 1.1 The interface traps are electrons or holes at the SiC/SiO_2 interface that are in direct communication with the semiconductor. Their charge state depends on the band bending at the interface and is assumed to follow the R-G process, see fig. 1.2 In I. the electron (filled circle) looses energy and is trapped by the R-G center potential, now a hole (outlined circle) is attracted by the electron. The hole looses energy and the two annihilate each other. In II. the the electron looses energy a second time and and the electron and hole annihilate one another. These processes result in the release of thermal vibrations in the crystal lattice, also known as a heat phonon (6)(12). Due to the wide-ranging and degrading effect on the operational behavior of MOS devices the interfacial traps at the MOS interface must be considered to be the leading contributor to the ideality deviation in these devices.
The time it takes for a electron to be emitted from the semiconductor valence band is usually referred to as the *emission time* labeled τ_c and the *emission rate* C_n is its inverse and is defined:

$$C_n = \sigma_n \nu_{th} n \tag{1.1}$$

where σ_n is the carrier capture cross section , ν_{th} is the carrier thermal velocity and n is the carrier density. It is clear that the thermal velocity and electron concentration are affected by temperature. The process of electron emission from a trapped state

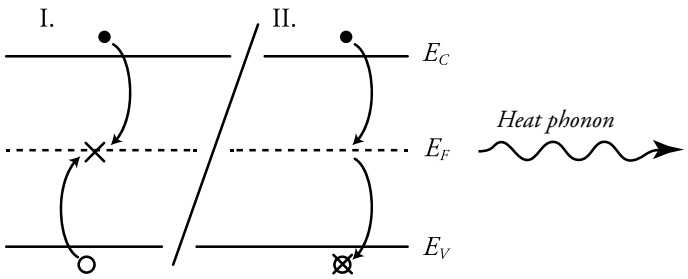

Figure 1.2: The Recombination - Generation process (R-G) or Shockley–Read–Hall (SRH) process. The conduction band energy is labeled E_C, valence band energy is E_V and the impurity introduced energy level is E_T. In I. the electron and hole annihilate one another at the fermi level, whereas in II. the electron travels down to the valence level and there the electron-hole annihilation takes place.

is characterized by:

$$e_n = \nu_{th}\sigma_n N_C e^{-\Delta E/k_B T} \tag{1.2}$$

here ΔE is the first order approximation for the depth of the interface state with respect to the conduction band of SiC, k_B is the Boltzmann constant and T is the absolute temperature. Measurements of the trap emission time at different temperatures make it possible to calculate the activation energy often assuming that σ_n is constant,. Normally

$$\sigma_n \sim 10^{-15} - 10^{-17}\text{cm}^2$$

for interface states and

$$\sigma_n \sim 10^{-17} - 10^{-20}\text{cm}^2$$

for traps witihn the oxide (6) (7).

Since the interface traps can be seen as a shift in the flat-band voltage in C-V curves the most common technique for characterization of shallow interface traps is capacitance-voltage (C-V) measurements. This technique has the advantage of being fast, each measurement takes only a few minutes. However when the C-V technique is used at room temperature, the investigative energy range is quite limited where the possible frequency span of the measurement decides how wide the interval will be. To paint a clearer picture of the interface states one needs to perform time consuming C-V measurements at different temperatures to gain access to slower traps who tend to have higher values for ΔE. At relatively high temperatures (250 K) the traps capable of emptying their charge by thermal emission in the 77 K - 250 K range, are fast enough to follow the gate voltage sweep. As opposed to 77 K where where the trapped charges are frozen in and thus unable to escape within the timeframe of the measurement, the key factor here is that the electron capture is normally very fast (large σ_n) while electron emission is slow (dependant on ΔE). This can be seen in C-V measurements as an additional negative fixed charge and the

corresponding flat-band voltage (V_{FB}) shift of the C-V curve. Then ΔV_{FB} provides an estimate of the density of the effective trapped charge at the SiC/SiO_2 interface (2). It is also possible to make a back and forth sweep an thereby get two C-V curves which are separated by a hysteresis, which comes from the afore mentioned processes of charge trapping. From there one can estimate the total number of trapped charges at a given voltage (8).

1.2.2 Samples

The measurements were made on four types of n-type 4H SiC MOS capacitors, all from different fabrication techniques.
In the sample we will refer to hence forth as TEOS the oxide is deposited at 985 K using tetraethyl orthosilicate. Prior to oxide deposition the native oxide was removed by hydroifluoric acid (HF). This TEOS process is at such a low temperature that negligible thermal oxidation of the SiC surface takes place. The TEOS oxide thickness is 95 nm with a surface area of ~ 70 nm^2
X797 and HL0542 are SiC samples that are thermally oxidized at 1150C for 48 hours resulting in an oxide thickness of ~ 170 nm for both samples. The measured surface areas were ~ 70 nm for the HL0542 sample and ~ 126 nm for X797. The only difference between the samples is the growth rate of the epitaxial layer that is underneath the thermal oxide. The HL0542 is grown using chlorine based hot wall chemical vapor deposition (CVD) with growth rate of 30 micrometers per hour. The X797 sample was grown by conventional CVD process with growth rate of 1-2 micrometers/hours.
And lastly we measured a sample to whom we will refer to as CONT. This sample was oxidized using sodium enhanced oxidation (SEO). The oxide growth rate in the presence of sodium is approximately tenfold compared to conventional thermal oxidation. Samples of this kind are virtually free of interface states. Here the oxide thickness is 91 nm ~ 70 nm^2 and the surface area of the contact ~ 70 nm^2.

1.2.3 Measurement techniques

We utilized three different C-V measurement methods in our attempt to characterize the shallow interface traps of the four samples. First we measured the capacitance versus voltage at different frequencies, ranging from 1 kHz to 1 MHz, at biases ranging from -10 V to 20 V, here we were able to get a sense of the distribution of interface traps. Next we made C-V measurements at ever increasing temperatures. We applied a negative bias to the sample, cooled it and made a front - back sweep C-V measurement at -10 V to 20 V, creating a hysteresis in the measurement. This was done on a temperature range of 77 K to 300 K. This was however only done

on the TEOS, HL0542 and X797 samples. Lastly we measured the C-V relationship when the sample was cooled from room temperature down to 77 K while maintaing a certain charging voltage. Then sequentially sweeping the bias from negative bias to increasing forward bias, for charging voltages from 0 V to 20 V. These three methods allowed us to determine the effective trapped charge at the SiC/SiO_2 interface.

1.3 Results and discussion

1.3.1 CV vs. frequency

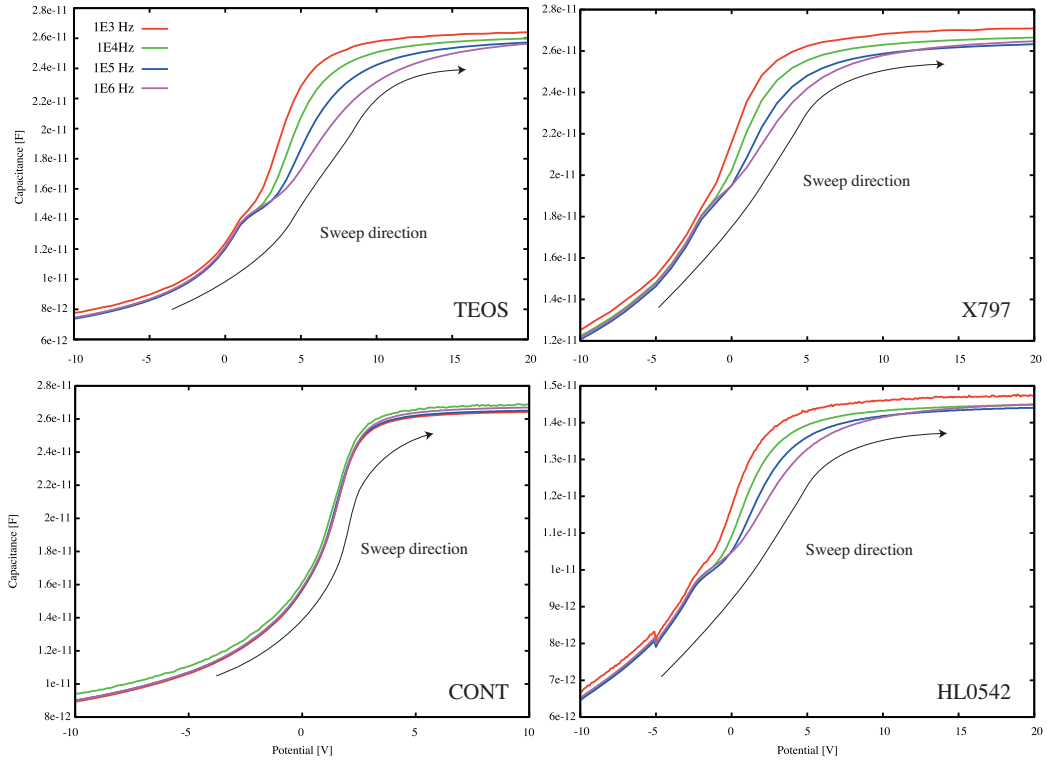

Figure 1.3: C-V at different frequencies. The gate bias is swept from negative to positive voltage

It is possible to evaluate the density of interface states by comparing high and low probing frequency C-V measurements. Here it is assumed that for a low probing signal interface states at or around the Fermi-energy will contribute to the capacitance signal, but for a high frequency probing signal the interface states will not contribute to the capacitance. This is due to the fact that the interface traps have emission rates of the same order as the probing signal whereas the deeper traps

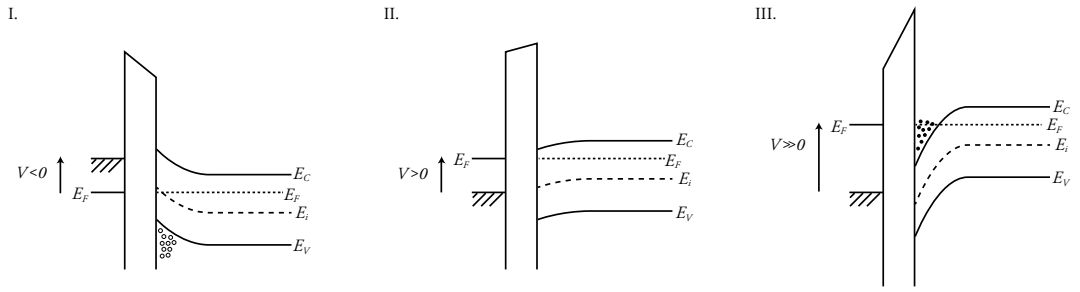

*Figure 1.4: E_F is the semiconductor Fermi level, E_C the conduction band energy level and E_V the valence energy level. Electrons are represented by filled circles and holes by outlined circles. **I.)** Negative gate voltage.**III.)** Small positive gate voltage. **IV.)** Large positive gate voltage.*

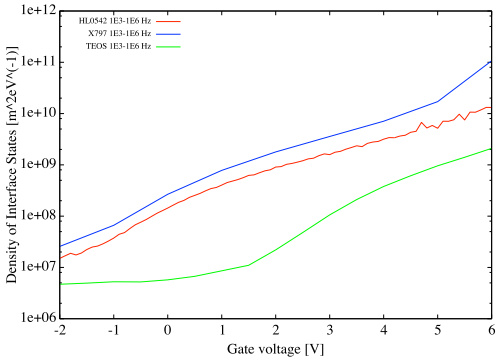

Figure 1.5: Density of interface states vs. voltage

have emission rates which are slower then the rate of the measurement itself. The frequency spectra for the samples can be seen in fig. 1.3. At negative gate biases, part I. of fig. 1.4, the energy bands of the semiconductor swerve upwards, no current flows over the device, assuming the device behaves close to ideality the Fermi level of the semiconductor is constant. Now due to the band bending holes accumulate at the SiO_2/SiC interface. At a low positive gate voltages , II. fig. 1.4, the energy bands bend downwards and the number of holes at the interface is diminished. The holes move away from the interface leaving a carrier-free zone at the interface laced with ionized carriers. When the gate voltage is increased further, part III. of fig 1.4, the band bending increases and E_F intersects with the partially falls within the conduction band of the semiconductor and charges accumulate at the interface (13). From the frequency spectra it was possible to establish the gate oxide capacitance (C_{ox}) and in conjunction with equation 3:

$$D_{IT}(V) = \frac{C_{ox}}{e_q}\left(\frac{C_{lf}/C_{ox}}{1 - C_{lf}/C_{ox}} - \frac{C_{hf}/C_{ox}}{1 - C_{hf}/C_{ox}}\right) \tag{1.3}$$

where e_q is the elementary charge, C_{lf} is the capacitance at 1 kHz and C_{hf} is the capacitance at 1 MHz. We were able to plot the density of states as a function of voltage (7) (9). The results can be seen in fig. 1.5. The capacitance difference in the CONT sample was to small to estimate the D_{it} for that sample so these results are omitted from fig 1.5. However there seems to be some difference in interface states between (the right side of the figure) the HL0542 sample and X797 sample despite the similarity in fabrication techniques. The TEOS sample results indicated that most of the interface states were present close to the SiC/SiO_2 interval. However most of the voltage range is not useful. The results are only reliable when the sample is accumulated.

1.3.2 CV at different temperatures

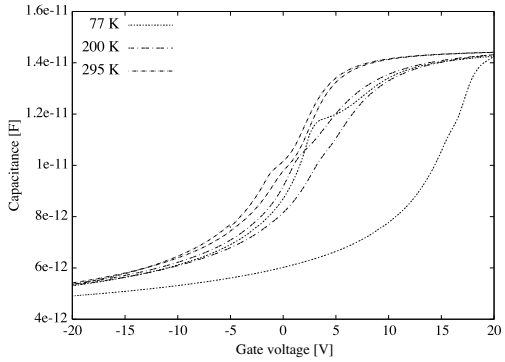

Figure 1.6: HL0542 C-V front and back sweep at different temperatures

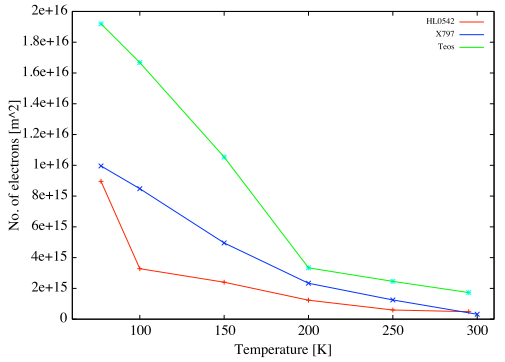

Figure 1.7: Number of trapped charges vs. temperature

In fig. 1.6 the results from the C-V at different temperatures for HL0542 are shown, the measurements on the other samples resulted in similar figures. The surface area

of the hysteresis was calculated and the number of trapped charges was estimated via eq. 4.

$$C = \frac{Ae_q n_q}{V} \tag{1.4}$$

Where A is the surface area ot the capacitor, e_q is the elemental charge, n_q is the number of trapped charges and V is the voltage. That number was then plotted with temperature, see fig 1.7. Here the difference between HL0542 and X797 was still present and the number of trapped charges in the HL0542 sample differed somewhat from the X797. Now the TEOS device and the X797 device portrayed similar behavior.

1.3.3 Electron trapping in interface states with increasing field across the oxide

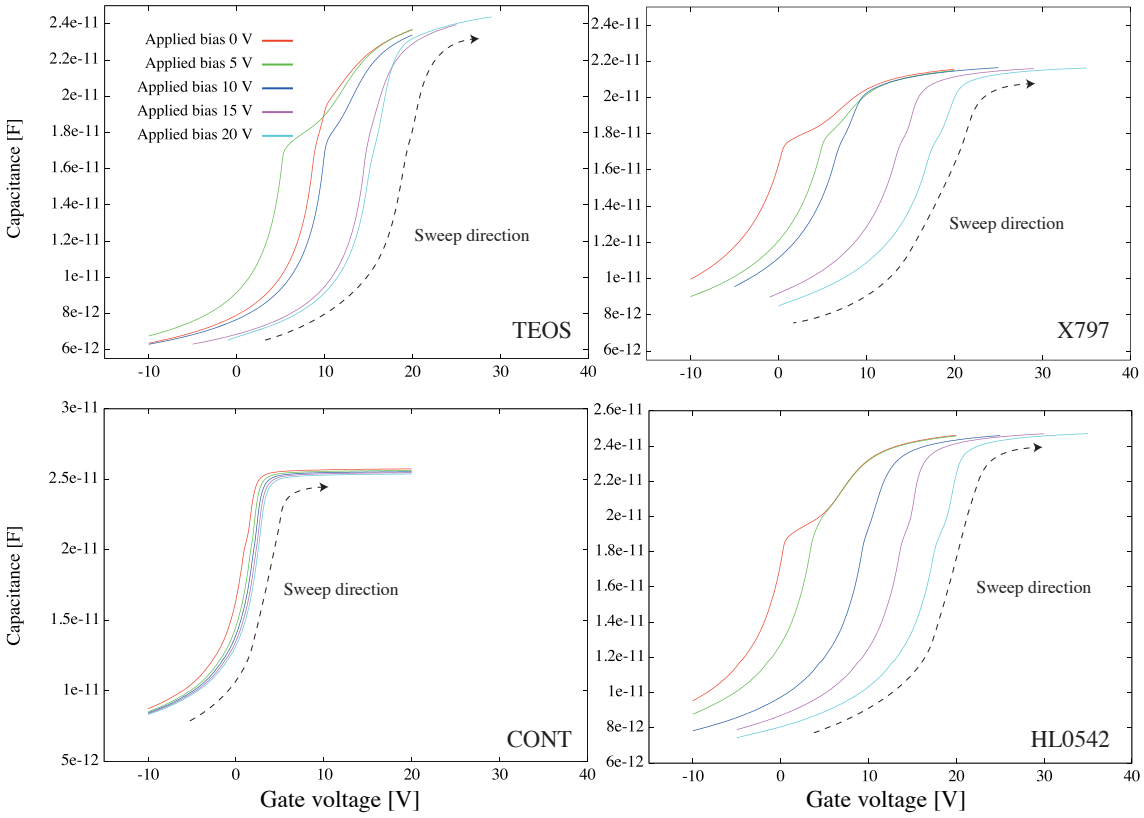

Figure 1.8: C-V at different gate voltages

We have already concluded that the interface traps thus far investigated can be seen as as shift in the flat band voltage in C-V curves measured at high and low temperatures. At room temperature the traps capable of emptying their charge by

thermal emission in the 77 - 300 K range are fast enough to follow the gate voltage sweep . But these same traps at 77 K are unable to emit their captured electrons within the timeframe of the measurement, effectively freezing the electron in the trap. By applying an incrementally increasing charging voltage it is possible to fill traps with an ever increasing energy. So the increased remaining charge can be seen as an increases in the C-V curve shift(2). Figure 1.8 shows the results from the C-V sweeps with subsequently increasing charge voltage. We estimated the flat-band voltage for each of the MOS capacitors (V_{FB}) using:

$$V_{FB} = \phi_{ms} - \frac{Q_f + Q_{0it} + \gamma Q_m}{C_{ox}} \tag{1.5}$$

where ϕ_{ms} is the work function difference, Q_f is the fixed oxide charge, Q_{it} is the charge trapped in the interface state at flat-band conditions an γQ_m, Q_f and γQ_m are constants. is the mobile charge weighted according to its distribution through the bulk of the oxide. Only Q_{it} is a function of gate voltage, The results of this comparison can be found in table 1.1. Again there was a clear difference between the HL0542 and X797 samples, which was represented itself as a difference in trapped charges at different field intervals. However the total trapped charge in both samples was comparable. The TEOS sample displayed similar behavior as before as well as the CONT sample. (7).

Table 1.1: Trapped charge at increasing electric field intervals.

	0-5 V	5-10 V	10-15 V	15-20 V	0 -20 V
TEOS	$5.87 * 10^{-11}$ Q	$-7.82 * 10^{-11}$ Q	$-8.16 * 10^{-11}$ Q	$-1.36 * 10^{-11}$ Q	$-11.47 * 10^{-11}$ Q
X797	$-7.48 * 10^{-11}$ Q	$-3.23 * 10^{-11}$ Q	$-1.21 * 10^{-10}$ Q	$-5.59 * 10^{-11}$ Q	$-28.4 * 10^{-11}$ Q
HL042	$-5.27 * 10^{-11}$ Q	$-1.02 * 10^{-10}$ Q	$-7.31 * 10^{-11}$ Q	$-6.8 * 10^{-11}$ Q	$-30.03 * 10^{-11}$ Q
CONT	$-1.36 * 10^{-11}$ Q	$-6.8 * 10^{-12}$ Q	$-3.4 * 10^{-12}$ Q	$5.1 * 10^{-12}$ [Q]	$-2.89 * 10^{-11}$Q

2 Conclusions

Using these three C-V techniques we have mapped out the shallow interface states in some detail. We have concluded that the interface traps in the TEOS sample are mostly accumulated near the interface. However to get a real sense of the interfacial traps at the SIC/SiO_2 interface more powerful and less time consuming methods are needed, f.ex. Deep Level Transient Spectroscopy (DLTS) (10). Nevertheless we have concluded that the interfacial states which are present at the semiconductor/insulator interface in the MOS capacitors we worked with are mostly present close to the interface itself, in order for the SiC/SiO_2 technology to become a viable alternative to the dominant Si/Sio_2 interfaces these traps need to be passivated with greater accuracy. The passivation in the CONT sample was somewhat successful as can be seen from the results, but the practical applications of sodium enhanced MOS devices is not feasible(11).

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