Investigation of interface and near-interface traps in silicon carbide MOS-capacitors using capacitance and conductance techniques

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INVESTIGATION OF INTERFACE AND NEAR-INTERFACE TRAPS IN SILICON CARBIDE MOS-CAPACITORS USING CAPACITANCE AND CONDUCTANCE TECHNIQUES

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60 ECTS thesis submitted in partial fulfillment of a Magister Scientiarum degree in Physics

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This thesis is dedicated to my family and friends who have been greatly supportive throughout my years of study.
Abstract

For the past few years silicon carbide (SiC) has become a popular semiconductor for use in high voltage applications such as a power metal oxide semiconductor field effect transistors (MOSFETs). Unfortunately SiC does not come without its flaws. One of the major problems facing scientists is the very low mobility of charge carriers across the channel. This low mobility has been accredited to high density of electron traps at the interface of the semiconductor and the dielectric grown on top. Furthermore near-interface traps can cause leakage over the gate causing undesirable problems, though leakage current is not the focus of this thesis. In this thesis 4H–SiC MOS-capacitors with three differently prepared silicon dioxide (SiO₂) films. These films are dry thermal oxide and oxide annealed in N₂O or in the presence of Na. Furthermore aluminum nitride - silicon dioxide (AlN/SiO₂) stacks and aluminum oxide (Al₂O₃) dielectrics are investigated. Their interface and near-interface trap densities are determined using Hi/Lo capacitance measurements and distributed circuit model based on conductance measurements. The Hi/Lo capacitance method is used at different temperatures to reveal the presence of slow and fast traps. The findings suggest that SiC/SiO₂ interface has the highest density of interface traps while the AlN/SiC and Al₂O₃/SiC have lower densities. The near-interface traps results show that the dry oxide has a density around 10^{13} \text{ cm}^{-2} while the N₂O annealed has density of 4 \cdot 10^{12} \text{ cm}^{-2} and the best results are found in the oxide grown in the presence of Na with density of about 3 \cdot 10^{11} \text{ cm}^{-2}. The results from the conductance measurements suggest that the AlN/SiO₂ stack and Al₂O₃ have high gate leakage thus near-interface traps can’t be determined. SiO₂ has little to no leakage but shows response from near-interface traps in a form of conductance at strong accumulation.
Útdráttur

Á undanförnum árum hefur kísilkarbíð (SiC) orðið mun vinsælla til notkunar í hás pennu rafrásum. Hins vegar eru ýmis vandamál sem koma upp í SiC þar á meðal er lágur hreyfanleiki hleðslubera þegar einangrandi lag er ræktað á yfirborðið sem takmarkar straumgetu rafráðsmáranna. Þessi lági hreyfanleiki hleðslubera hefur verið rakinn til mikils þetitleika veilna á samskeytum SiC og einangrarans. Í þessu verkefni voru skoðaðir þettar sem búnir voru til í SiC þar sem einangrandi lagafélag, sem er á milli undirlagsins og málsins, var úr mismunandi efnum og ræktað með mismunandi aðferðum. Einangrarchitecture voru kisildíoxíð (SiO₂), þurrt oxíð og oxíð bakað í N₂O eða ræktað í nærveru Na, ániftríð og kisil díoxíð staflí (AlN/SiO₂) og álóxið (Al₂O₃). Hi/Lo ráðarmæliðferðar var notuð við að skoða veilur á samskeytum SiC og einangrarans. Nýlega tilkomið dreiftr rafráðslíkan var notað til að ákvarða þetitleika grannveilna við samskeytin. Næmni Hi/Lo ráðarmæliðferðararinnar er hítastigsháð og eru því gerðar nokkrar mælingar til að skoða hvernig þetitleikin breytist með hitastigi. Niðurstöðurnar benda til að SiO₂/SiC samskeytin hafi mjög mikinn veilupþetitleika á meðan veilupþetitleiki AlN/SiC og Al₂O₃/SiC samskeytanna er mun lægri. Þó er grannveilupþetitleikin lægstur fyrir oxíð ræktað við nærveru Na en hín sýnir og hæstur fyrir þurr oxíð sýnir. Leiðnimbældingarnar benda til að AlN/SiO₂ og Al₂O₃ hafi veilur sem leyfa smug í gegnum sig og valda lekastaum yfir hliðið en SiO₂ sýnir nánast enga leiðni annað en smug til grunnra veilna í oxíðinu.
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1. Introduction

Metal oxide semiconductor field effect transistor (MOSFET) is the main building block of all modern logic technology. MOSFETs are commonly made with silicon (Si) but in recent years power MOSFETs have been introduced in silicon carbide (SiC). SiC has a large energy bandgap which makes the material applicable for high voltage and high temperature applications. However SiC MOSFETs devices are currently hampered by low inversion channel mobility which is due to high defect density at the interface between SiC and the native gate oxide (SiO$_2$). The first SiC commercial wafers were made in the 1997 and six inch wafers were introduced by Cree in 2012 [15].

1.1. SiC crystal structure and properties

SiC has many different crystal structures but for research and development purposes the hexagonal structures, 4H-SiC and 6H-SiC, are the most common. In the crystal structure of SiC, the nearest neighbour (NN) of every silicon atom is a carbon atom and every NN of carbon atom is a silicon atom and they are bounded with the sp$^3$ orbitals, this is schematically shown in figure 1.1.

![Atomic structure of SiC. On the left silicon atom with four carbon NN and to the right a carbon atom with four silicon NN.](image)

The planar configuration of atoms in the SiC bulk can be either AB or AC stacked. Meaning, if Si atoms are on the bottom of the stack in the plane, carbon atoms can have two configurations stacking on top as can be seen in figure 1.2. When the wafer is produced, the cut is made through the slab along the (0001) plane at a 4° off-axis
1. Introduction

tilt seen in figure 1.3. That face is called the Si-face. This off-axis tilt is needed for proper epitaxial layer growth.

![Figure 1.2: Planar stacking structure in bulk SiC. On the left AB stacking and on the right AC stacking.](image)

The metal oxide semiconductor capacitors (MOS-capacitors) used in this thesis are all made on the silicon-face of the wafer. The stacking of planes in the SiC bulk differ between the 4H-SiC and the 6H-SiC. The 4 and 6 represent the number of stacks before the stacking repeats itself, example ACAB in 4H-SiC and ABCACB in 6H-SiC.

![Figure 1.3: The 4° off-axis cut of 4H-SiC made for epitaxial growth [18]. The surface of this cut would be the Si-face](image)

Table 1.1 compares the physical properties of SiC and Si. Higher thermal conductivity and electron saturation velocity in SiC allows SiC devices to operate at higher temperatures and higher frequencies, while silicon becomes intrinsic above 250°C. The high breakdown field in SiC also makes it ideal for high voltage and high power applications.

Table 1.1: Comparison of physical properties of bulk silicon, 4H-SiC and 6H-SiC at room temperature [16].

<table>
<thead>
<tr>
<th>Property</th>
<th>Silicon</th>
<th>4H-SiC</th>
<th>6H-SiC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Energy bandgap [eV]</td>
<td>1.1</td>
<td>3.26</td>
<td>3.0</td>
</tr>
<tr>
<td>Dielectric constant</td>
<td>11.9</td>
<td>9.7</td>
<td>9.7</td>
</tr>
<tr>
<td>Bulk e− mobility [cm²/Vs]</td>
<td>1350</td>
<td>880</td>
<td>360</td>
</tr>
<tr>
<td>Saturation velocity [cm/s]</td>
<td>10⁷</td>
<td>2.2·10⁷</td>
<td>2.5·10⁷</td>
</tr>
<tr>
<td>Breakdown field [MV/cm]</td>
<td>0.25</td>
<td>2.2</td>
<td>2.5</td>
</tr>
<tr>
<td>Thermal conductivity [W/cm K]</td>
<td>1.5</td>
<td>5.0</td>
<td>5.0</td>
</tr>
</tbody>
</table>
1.2. Gate dielectrics

SiC, thanks to its large bandgap, has promising qualities for use in high power applications. However growing gate dielectrics on SiC is a challenge and the main obstacles are low inversion channel carrier mobility due to electron scattering at the SiC/dielectric interface, charge trapping and trap assisted tunneling [10, 19]. In this thesis three different types of gate dielectrics on 4H-SiC are explored and their interface trap density ($D_{it}$) and near-interface trap density ($N_{bt}$) is modeled.

Silicon dioxide ($\text{SiO}_2$) is the most commonly used dielectric and can be grown uniformly on the surface of the SiC wafer by thermal oxidation. SiO$_2$ has a 9 eV bandgap with 2.7 eV and 3.05 eV offsets to conduction and valence band respectively on 4H-SiC [19]. In dry oxidation the following reactions occurs [25]:

$$\text{SiC} + \frac{3}{2}\text{O}_2 \leftrightarrow \text{SiO}_2 + \text{CO}$$

$$\text{SiC} + \text{O}_2 \leftrightarrow \text{SiO}_2 + \text{C}$$

Excess carbon left in the oxide is determined by the reactions

$$\text{SiC} + 2\text{CO} \leftrightarrow 3\text{C} + \text{SiO}_2$$

$$2\text{C} + \text{O}_2 \leftrightarrow 2\text{CO}.$$  

It is commonly assumed that most of the carbon is removed from the SiC/SiO$_2$ interface as CO gas. But it has been hypothesized that carbon forms clusters and

![Energy band diagram of a MOS-capacitor. At the interface there are interface traps (IT) and inside the dielectric there are near-interface traps (NIT). Electrons are captured by the ITs and NITs.](image)

It is commonly assumed that most of the carbon is removed from the SiC/SiO$_2$ interface as CO gas. But it has been hypothesized that carbon forms clusters and
dangling bonds at the SiC/SiO$_2$ interface and causes high number of interface traps [6, 13] as shown schematically in figure 1.4. Such possible carbon related interface defects should be less apparent in deposited oxide but experimental data of deposited oxides shows comparable interface defect densities. In addition it has been observed that carbon is injected into the SiC during thermal oxidation [11].

In figure 1.5 the trap density vs. energy at the interface is schematically shown. Close to the interface the oxide provides traps about 2.8 eV below the SiO$_2$ conduction band edge. These traps are acceptor-like since they are neutral when they are empty. When the Fermi-level approaches the SiC conduction band edge electron trapping occurs. The high density of traps near the conduction band are the cause of the very low channel mobility in 4H-SiC n-channel MOSFETs.

The high density of interface traps close to the conduction band has been a major obstacle is development of MOS devices. Therefore attempts have been made to improve the SiC/SiO$_2$ interface with a variety of methods such as:

- Complete or partial growth of the gate oxide in a presence of nitrogen containing gas (NO or N$_2$O). The NO and N$_2$O dissociates at very high temperature (1200°C) and atomic nitrogen released makes a strong Si-N bond at the interface that neutralizes the interface traps. The results of introducing N-gas to the growth process has been shown to reduce the density interface traps and improve the carrier mobility [6].

- Direct deposition of the SiO$_2$ on the SiC using remote plasma enhanced chemical vapor deposition (PECVD) or jet vapor deposition have been tried but the results are not satisfactory [13].

- Post-oxidation annealing with pyrogenic stream (H$_2$+O$_2$) at temperature below the oxidation temperature of SiC reduces the density of deep interface traps but increases the density of shallow traps that limit the carrier mobility [13].
1.3. The MOS Capacitor

The nitridation technique has been successful in reducing the interface traps and has led to commercially available high voltage (>900 V) SiC MOSFETs. Commercial SiC MOSFETs mostly use nitrided oxides. These high voltage devices can function at lower mobilities than the lower voltage devices because the current is limited by the resistance of the low doped epitaxial layer in the high voltage devices.

**Aluminum oxide** (Al$_2$O$_3$) can be grown on SiC wafers with many different techniques such as plasma deposition and atomic layer deposition (ALD) [13]. Al$_2$O$_3$ has a bandgap of 7.0 eV with 1.6 eV and 2.14 eV offsets to conduction and valence band respectively on 4H-SiC [5, 8, 20].

**Aluminum nitride** (AlN) has the smallest bandgap of all the dielectrics used in our experiments or only 6.2 eV with 1.7 eV and 1.3 eV offsets to the conduction and valence band respectively on 4H-SiC [1, 9, 20, 22, 23].

1.3. The MOS Capacitor

The typical MOSFET structure has drain, source, gate and body terminals, as can be seen in figure 1.6. To the left in figure 1.6 is a typical MOSFET structure and to the right is the heart of the MOSFET, the gate structure that forms the MOS-capacitor. Other types of MOSFET structures, such as trench gate structures have shown promising results in terms of enhanced carrier mobility that is due to the channel is no longer on the (0001) plane of the SiC but on the (11-20) plane where the interface trap density is lower [18].

![MOSFET diagram](image)

*Figure 1.6: On the left is planar MOSFET structure with gate length L and on the right is the heart of the MOSFET the MOS-capacitor.*

The function of ideal n-channel MOSFET is in principle straight forward. In equilibrium with no voltage applied the energy bands are flat, figure 1.7.b). When
positive voltage is applied to the gate, electric field is created over the oxide thus pulling electrons from the substrate up to the oxide-semiconductor interface and going into depletion, see figure 1.7.c). When the electric field is strong enough the MOS-capacitor goes into inversion, as indicated in figure 1.7.d). To conduct current between the source and the drain a voltage is applied on the drain, creating electric field pointing from drain to source, and electrons flow from the source to the drain.

![Diagram of MOS-capacitor energy bands](image)

**Figure 1.7**: Ideal p-type MOS-capacitor energy band diagram. $\phi_m$ is the work functions of the metal and $\chi_s$ is the electron affinity in the SiC. a) Band diagram in accumulation $V < 0$. b) Band diagram at flat band $V = 0$. c) Band diagram in depletion $V > 0$. d) Band diagram in inversion $V > 0$.

In the MOS-capacitor the energy bands follow the same process as described earlier for the MOSFET. But in SiC there is one difference: inversion is never reached in SiC MOS-capacitors because of insignificant minority carrier generation at room temperature. Making a MOSFET takes much longer time and is far more demanding than making only the MOS-capacitor. Since the main challenges are with the carrier mobility over the gate channel and the main reason for low mobility has been accredited to interface traps it makes more sense to only produce the MOS-capacitor and investigate the interface trap density, thus saving time for production processes and research.
2. Experimental method

2.1. Samples

In this thesis SiO\(_2\), AlN/SiO\(_2\) stack and Al\(_2\)O\(_3\) dielectrics, grown on Si-face 4H-SiC with 4° off-axis cut are investigated. All samples are circular MOS-capacitor structures with radius of 150 \(\mu m\). The SiO\(_2\), AlN/SiO\(_2\) and Al\(_2\)O\(_3\) samples are prepared on n-type epitaxial layers grown on highly doped substrate with net doping concentration of \(10^{18}\) cm\(^{-3}\). The epitaxial layers are 10 \(\mu m\) thick with net concentration \(10^{16}\) cm\(^{-3}\). The gate metal is Al and the backside contact is made by thick Ni (100 nm) or Al (500 nm) metallization [13].

Table 2.1: Methods used to grow the dielectric films in this thesis.

<table>
<thead>
<tr>
<th>Sample</th>
<th>Thickness</th>
<th>Growth method</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiO(_2) B6</td>
<td>43 nm</td>
<td>Dry thermal oxidation at 1150°C [4]</td>
</tr>
<tr>
<td>SiO(_2) F2</td>
<td>31.5 nm</td>
<td>Dry thermal oxidation at 1200°C [4]</td>
</tr>
<tr>
<td>SiO(_2)/N(_2)O</td>
<td>37.1 nm</td>
<td>Grown in N(_2)O ambient at 1240°C for 90 min [2]</td>
</tr>
<tr>
<td>SiO(_2)/Na</td>
<td>108 nm</td>
<td>Sodium enhanced oxidation (SEO) method. In this method, a 100nm SiO(_2) was grown in O(_2) ambient at 1240°C and densified in nitrogen medium at 1000°C for 5 hours [3].</td>
</tr>
<tr>
<td>AlN/SiO(_2)</td>
<td>50 nm</td>
<td>~10nm thick AlN grown on the SiC with MOCVD at 300°C and ~40nm thick SiO(_2) is grown on the AlN with PECVD at 1100°C [13].</td>
</tr>
<tr>
<td>Al(_2)O(_3)</td>
<td>15 nm</td>
<td>Grown by oxidation of Al using a hot plate at 200°C and is ~15 nm thick [12].</td>
</tr>
</tbody>
</table>

2.2. Capacitance and conductance measurements

All measurements are done with Agilent E4980A precision LCR meter by applying DC bias on the MOS-capacitor and adding small AC signal of 10mV to the DC bias using frequencies from 1kHz to 1MHz. The samples are mounted on a holder that
2. Experimental method

is placed inside of Janis Research VPF-800 liquid nitrogen cryostat, only exception
is the 44 K measurement on sample F2 which is done in a helium closed cycle cryo
chamber. Measurements are done at temperatures ranging from 44 K to 350 K.
Capacitance and conductance measurements are done simultaneously by the LCR
meter.

2.2.1. Interface Trap Density from CV Measurements

Capacitance vs. voltage (CV) measurements are the most common way to investi-
gate MOS-capacitors. From the CV measurements we extract the oxide thickness
\( t_{ox} \), flatband voltage \( V_{FB} \), oxide capacitance \( C_{ox} \) and doping concentration \( N_D \), of
the epilayer.

In figure 2.1(a) the sweep begins with a negative voltage bias applied to the n-
type capacitor, this will push the electrons from the SiC/SiO\(_2\) interface into the
substrate and create a depletion region. Sweeping the gate from negative to positive
the capacitance gets higher and in the region of steep climb of capacitance is the
flatband capacitance/flatband voltage. Sweeping to higher voltage will accumulate
electrons at the interface and the only visible capacitance is the dielectric capacitance
called \( C_{ox} \). There is a dispersion in the capacitance at different frequencies. This
dispersion is due to the response from traps at the SiC/SiO\(_2\) interface. Traps closer
to the conduction band in the SiC will response faster than deeper traps further
away from the conduction band edge.

From figure 2.1(b) we extract the flatband voltage and the slope in depletion to
calculate the doping concentration of the epilayer with equation 2.1.

\[
N_D = \frac{2}{q_e \epsilon_0 \epsilon_{ox} A^2 \frac{d\left(1/C^2\right)}{dv}}
\]

(2.1)

Where \( q_e \) is the electron charge, \( \epsilon_0 \) and \( \epsilon_{ox} \) are the permittivity of vacuum and the
oxide respectively and \( A \) is the area of the capacitor.

The thickness of the oxide can be calculated as

\[
t_{ox} = \epsilon_0 \epsilon_{ox} \frac{A}{C_{ox}}
\]

(2.2)

where \( C_{ox} \) is the highest capacitance in strong accumulation as in figure 2.1(a).
2.2. Capacitance and conductance measurements

![Graph](image)

**Figure 2.1:** Capacitance and $1/C^2$ as functions of gate voltage. (a) The room temperature sweep of sample B6; (b) $1/C^2$ of the data to the left with best line through it to find the flatband voltage and the slope, $d(1/C^2)/dV$, to calculate the doping concentration.

With Hi/Lo capacitance measurement we extract the density of interface traps ($D_{it}$) in the forbidden band gap of the SiC using the expression [17].

$$D_{it} = \frac{C_{ox}}{q_e} \left( \frac{C_{lf}/C_{ox}}{1 - C_{lf}/C_{ox}} - \frac{C_{hf}/C_{ox}}{1 - C_{hf}/C_{ox}} \right)$$  \hspace{1cm} (2.3)

Where $C_{lf}$ and $C_{hf}$ is the capacitance at the lowest and highest frequencies used to measure respectively. To find the band bending the measured CV data is compared to the small signal capacitance of a theoretical ideal MOS-capacitor as described by [25].

$$C_s = -sgn(\phi_s) \sqrt{\frac{q_e \epsilon_s \epsilon_0 N_D}{2}} \frac{1 - e^{\phi_s/\phi_t}}{\sqrt{\phi_t e^{\phi_s/\phi_t} - \phi_t - \phi_s}}$$  \hspace{1cm} (2.4)

where $\phi_s$ is the band bending, $\phi_t = k_B T/q_e$, where $T$ is the temperature, $k_B$ is the Boltzmann constant and $\epsilon_s$ the the permittivity of the SiC. The offset energy from bottom of the conduction band in the SiC to the interface trap is calculated using

$$\Delta E = E_c - E_T = E_F - \phi_s$$  \hspace{1cm} (2.5)

where $E_c$ is the energy of the conduction band in the SiC, $E_T$ is the trap energy and $E_F$ is the Fermi energy level.
2. Experimental method

Figure 2.2: Estimation of band-bending $\phi_s$ as function of gate voltage. a) The CV data from measurements; b) The theoretical calculations of the capacitance as function of band-bending; c) Band-bending as function of gate voltage; d) $\phi_s$ vs. $\phi_s$.

The energy interval that’s valid for investigation is calculated using

$$e_m = N_c v_{th} \sigma e^{-\frac{E}{k_B T/q_e}}$$

(2.6)

where $e_m$ is the emission rate of electrons from traps, $N_c$ is the effective density of states in the conduction band, $v_{th}$ is the thermal velocity, $\sigma$ is the capture cross section of electrons, we chose $\sigma = 1.5 \cdot 10^{-15}$ cm$^{-2}$ which is a typical experimental value for interface traps, and $E$ is the valid energy matching the emission rate.

As can be seen from equation 2.6 the emission rate from traps is highly dependent on temperature thus measurements are done at temperatures ranging from 44 K to 350 K. Lower temperature will allow us to detect very fast traps that can’t be seen at room temperature and high temperature will allow us to detect very slow traps.
2.2. Capacitance and conductance measurements

2.2.2. Near-Interface Trap Density from GV Measurements

Conductance measurements have been used to obtain the density of near-interface traps \((N_{bt})\) [14]. Such measurements are done here on the same samples as for the capacitance measurements with the same equipment as described before. In figure 2.3 a typical peak appears around the flatband voltage which is due to the response from interface traps near the Fermi level. In strong accumulation the conductance is non-zero. Under strong accumulation the Fermi level at the SiC/SiO\(_2\) interface is either very close to or above the conduction band edge of the SiC. The non-zero conductance was first assumed to be series resistance \((R_s)\) but recent studies have shown that this conductance is due to tunneling to and from near-interface traps \((NITs)\) inside the oxide \([21, 24]\). By using this non-zero region of the conductance spectra we can estimate the density of near-interface traps.

![Conductance sweep data of sample B6 at room temperature with frequencies ranging from 1kHz to 1MHz. Higher frequency is more effected by series resistance thus the conductance in strong accumulation is higher.](image)

The distributed circuit model described in \([21]\) is used to determine the near-interface trap density and the circuit proposed is shown in figure 2.4. The model described assumes that the NITs are distributed throughout the oxide and adds the effects of each trap to the conductance and capacitance up to the total admittance of the MOS-capacitor. The admittance of the MOS-capacitor is expressed as

\[
\frac{dY}{dx} = -\frac{Y^2}{j\omega \epsilon_{ox}} + \frac{q^2 N_{bt} \ln(1 + j\omega \tau_0 e^{2\kappa x})}{\tau_0 e^{2\kappa x}} \tag{2.7}
\]

\[Y(x) = G_{tot} + j\omega C_{tot} \tag{2.8}\]

where \(G_{tot}\) and \(C_{tot}\) are the total conductance and capacitance of the MOS-capacitor, \(x\) is the distance from the SiC/SiO\(_2\) interface into the oxide dielectric, \(\omega\) is the angular frequency, \(\tau_0\) is the trap time constant at the interface and \(\kappa\) is the tunneling attenuation coefficient of the electron wave-function with energy \(E\) and is written as
2. Experimental method

Figure 2.4: Modeling the electric circuit of a MOS-capacitor to determine the density of near-interface traps [24].

\[ \kappa = \sqrt{2m_e^*(E_{ox} - E)} \frac{\hbar}{h} \]  

(2.9)

where \( m_e^* \) is the effective mass of an electron within the oxide and \( E_{ox} \) is the gate dielectric energy barrier height offset to the SiC conductance band.

Figure 2.5: Extraction of \( R_s \) from sample B6 by plotting \( G_m/\omega C_m^2 \) against angular frequency at bias voltage of 9V.

The analytical solution to equation 2.7 on matlab form is borrowed from [7] but the process of finding the \( N_{bt} \) has been automated and is shown in appendix A.2.

The total conductance signal in strong accumulation is mainly of two contributions, one from the NITs which is approximately proportional to the frequency and then a term due to series resistance which behaves as frequency squared [24]. \( R_s \) has great impact on the conductance and has to be corrected for, thus only conductance in the GV spectra will be due to NITs. The \( R_s \) is extracted by plotting \( G_m/\omega C_m^2 \) against frequency where \( G_m \) and \( C_m \) are the measured values of conductance and
2.2. Capacitance and conductance measurements

capacitance of the MOS-capacitor at high accumulation. Example of this is shown in figure 2.5 for sample B6.

The correction for $R_s$ of the conductance spectra is expressed as [14]

$$G_c = \frac{(G_m^2 + \omega^2 C_m^2)a}{a^2 + \omega^2 C_m^2}$$

(2.10)

where $a = G_m - (G_m^2 + \omega^2 C_m^2)R_s$. 
3. Results and Discussion

Table 3.1 shows summary of the results for using the Hi/Lo capacitance method and the distributed circuit model using conductance to determine the $D_{it}$, $N_{bt}$, flatband voltage and series resistance.

<table>
<thead>
<tr>
<th></th>
<th>B6 1150°C</th>
<th>F2 1200°C</th>
<th>SiO$_2$-Na</th>
<th>SiO$_2$-N$_2$O</th>
<th>AlN/SiO$_2$</th>
<th>Al$_2$O$_3$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$D_{it}$ [cm$^{-2}$eV$^{-1}$]</td>
<td>5.5·10$^{11}$</td>
<td>5.0·10$^{11}$</td>
<td>9.7·10$^{10}$</td>
<td>5.7·10$^{11}$</td>
<td>2.0·10$^{11}$</td>
<td>1.1·10$^{11}$</td>
</tr>
<tr>
<td>$N_{bt}$ [cm$^{-2}$]</td>
<td>8.6·10$^{12}$</td>
<td>1.5·10$^{13}$</td>
<td>2.7·10$^{11}$</td>
<td>4.1·10$^{12}$</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>$R_s$ [Ω]</td>
<td>2.048</td>
<td>1.464</td>
<td>0.005</td>
<td>1.152</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>$V_{FB}$ [V]</td>
<td>1.1</td>
<td>0.3</td>
<td>4.1</td>
<td>0.8</td>
<td>0.9</td>
<td>0.4</td>
</tr>
</tbody>
</table>

3.1. Results from CV data

The results of the Hi/Lo CV determining the $D_{it}$, of dry thermal oxide samples B6 and F2, are shown in figure 3.1 and the matlab code is shown in appendix A.1.. As expected the $D_{it}$ rises with lower energy, meaning the density of traps close to the conduction band of the SiC is higher as shown schematically in figure 1.5.

Looking at the CV measurements data for the samples in figures 3.1(a), 3.1(c) and 3.2 we see how the capacitance shifts with frequency of the AC signal. This shift is due to the energy of the traps responding to emission rate frequency described by equation 2.6 where the frequency of the AC signal takes the place of $e_m$. As it’s clearly visible in figures 3.1(a), 3.1(c) and 3.2(a) the frequency shift is quite large indicating high density of interface traps. Analyzing figures 3.2(b) 3.2(c) and 3.2(d) the frequency shift is barely visible indicating very low density of interface traps. The results for density of interface traps is shown in figure 3.3. There we see that B6 and F2 sample with SiO$_2$ dielectric are indeed with higher density of interface traps than the Na, AlN/SiO$_2$ and Al$_2$O$_3$ samples.

In figure 3.3 the results of Hi/Lo CV to determine the $D_{it}$ is shown for all samples tested at room temperature. As expected the dry oxides B6 and F2 have high $D_{it}$,
3. Results and Discussion

Figure 3.1: Capacitance measurements of B6 and F2 at room temperature and the results of $D_{it}$ calculations at different temperatures. (a) CV of sample B6 at room temperature; (b) Density of interface traps extracted from CV data at different temperatures for sample B6; (c) CV of sample F2 at room temperature; (d) Density of interface traps extracted from CV data at different temperatures for sample F2.

5.5 · $10^{11}$ cm$^{-2}$eV$^{-1}$ and 5.4 · $10^{11}$ cm$^{-2}$eV$^{-1}$ respectively. The SiO$_2$ annealed in N$_2$O has similar $D_{it}$, 5.0 · $10^{11}$ cm$^{-2}$eV$^{-1}$, as the dry oxides but the SiO$_2$ grown in the presence of Na sample has the lowest $D_{it}$ or 9.7 · $10^{10}$ cm$^{-2}$eV$^{-1}$. The AlN/SiO$_2$ and Al$_2$O$_3$ have $D_{it}$ 2.0 · $10^{11}$ cm$^{-2}$eV$^{-1}$ and 1.1 · $10^{11}$ cm$^{-2}$eV$^{-1}$ respectively.
3.1. Results from CV data

Figure 3.2: CV curves recorded at room temperature for samples with different dielectrics. (a) Capacitance measurement of SiO$_2$ annealed in N$_2$O; (b) Capacitance measurement of SiO$_2$ grown in presence of Na; (c) Capacitance measurement of AlN/SiO$_2$; (d) Capacitance measurement of Al$_2$O$_3$

Figure 3.3: Comparison of the density of interface traps at room temperature as function of energy difference between the SiC conduction band edge and the energy of the trap.
3. Results and Discussion

3.1.1. Capacitance dependence on temperature.

Dry thermal oxide sample B6 was swept at temperatures from 77 K to 298 K, sample F2 was swept at temperatures from 44 K to 350 K while AlN/SiO$_2$ and Al$_2$O$_3$ were measured at 77 K and 298 K. The results of the measurements are shown in figure 3.4. Analyzing figure 3.4 we see that all samples tested at different temperatures have some shift in flatband voltage. The dry thermal SiO$_2$ has significant shift while the AlN/SiO$_2$ and Al$_2$O$_3$ has very small shift. In figure 3.4(a) at a temperature of 125 K and under a hump appears and causes a much bigger shift in flatband voltage. This hump is due to traps with very distinctive energy that capture electrons and cause the capacitance curve shifts. A similar hump appears in figure 3.4(b) but at lower temperature or at 77 K.

![Figure 3.4: Capacitance sweeps of all samples at different temperatures at frequency of 1MHz: (a) Sample B6 at temperatures from 77 K to 298 K; (b) Sample F2 at temperatures from 44 K to 350 K; (c) Sample with AlN dielectric at temperatures 77 K and 298 K; and, (d) Sample with Al$_2$O$_3$ dielectric at temperatures 77 K and 298 K.](image-url)
In figure 3.5 we see how the CV curve shifts at different frequencies at 44 K for sample F2. This shift at different frequencies makes it impractical to use the Hi/Lo CV method to determine the $D_{it}$ because this shift will give much higher $D_{it}$ than is actually present in the sample. It is also not possible to use the 100 kHz curve which has as well a hump causing shift in the flatband voltage. The occurrence of such humps can limit the use of the Hi/Lo method. The humps are due to high density of interface traps within a very small energy interval.

![Figure 3.5: Capacitance sweep of sample F2 at 44 K at 4 different frequencies](image)

**3.2. Results from GV data**

The conductance spectra of the samples before and after correction are shown in figures 3.6 to 3.10 and the experimental data with the model fitting of the conductance are shown in figure 3.11.

The conductance spectra for the AlN/SiO$_2$ and Al$_2$O$_3$ are shown in figure 3.6. As we see in figures 3.6(a) and 3.6(b) the conductance does not go down after the flatband peak like expected that indicates a high leakage current though the AlN/SiO$_2$ and Al$_2$O$_3$ oxides. Thus using the distributed circuit model is impractical and results using the model couldn’t be trusted to determine the $N_{bt}$. But in figures 3.7 to 3.10 the flatband peak is clearly visible and as we see after the correction the conductance lowers in strong accumulation. The matlab program, shown in appendix A.2, runs through the calculations for the total admittance and finds the best fit to the corrected data of the conductance as seen in figure 3.11. Even though the fit is not perfect it’s close enough for the results to be reliable. The results can be seen in table 3.1.

Analyzing figures 3.7 to 3.10 we see clear flatband peak in all samples and no indication of leakage. We choose the voltage to extract our series resistance as 9 V, 8
3. Results and Discussion

V, 5 V and 5.5 V on samples B6, F2, N\textsubscript{2}O annealed and Na annealed respectively. Using equation 2.10 and extracting the series resistance we get 2.048 $\Omega$, 1.464 $\Omega$, 1.152 $\Omega$ and 0.005 $\Omega$ respectively. $R_s$ is very low for the Na annealed sample but that could be because the conductance is so low and so noisy that is very hard to find voltage range to extract the series resistance.

Figure 3.11 shows the fitting of the model to the conductance data for sample B6. This fit gives $N_{bd} = 8.6 \cdot 10^{12} \text{ cm}^{-2}$. For the other samples we get $1.5 \cdot 10^{13} \text{ cm}^{-2}$, $4.1 \cdot 10^{12} \text{ cm}^{-2}$ and $2.7 \cdot 10^{11} \text{ cm}^{-2}$ respectively.

Previous experiments on the samples B6, F2, SiO\textsubscript{2} annealed with N\textsubscript{2}O and SiO\textsubscript{2} grown in the presence of Na using TDRC are compared in table 3.2 [2, 4, 3]. TDRC measurements are performed by biasing the gate with fixed positive voltage, in the case of n-type substrate, to fill the interface and near-interface traps. The sample is cooled down to 30-40 K. When the sample has cooled down the bias is turned off and the electrons will retreat from the interface. This technique measures the current flowing from the interface while the sample is heated back up to room temperature and integration of the current curve provides an estimate of the total density of interface traps and near-interface traps within the sample.

<table>
<thead>
<tr>
<th>Sample</th>
<th>Model Torque</th>
<th>TDRC Torque</th>
</tr>
</thead>
<tbody>
<tr>
<td>B6</td>
<td>$8.6 \cdot 10^{12} \text{ cm}^{-2}$</td>
<td>in the high $10^{12} \text{ cm}^{-2}$</td>
</tr>
<tr>
<td>F2</td>
<td>$1.5 \cdot 10^{13} \text{ cm}^{-2}$</td>
<td>in the high $10^{12} \text{ cm}^{-2}$</td>
</tr>
<tr>
<td>SiO\textsubscript{2}/N\textsubscript{2}O</td>
<td>$4.1 \cdot 10^{12} \text{ cm}^{-2}$</td>
<td>$1 \cdot 10^{12} \text{ cm}^{-2}$</td>
</tr>
<tr>
<td>SiO\textsubscript{2}/Na</td>
<td>$2.7 \cdot 10^{11} \text{ cm}^{-2}$</td>
<td>$1 \cdot 10^{11} \text{ cm}^{-2}$</td>
</tr>
</tbody>
</table>
3.2. Results from GV data

![Graphs showing conductance vs gate voltage for different samples before and after correction at 1 kHz and 1 MHz.](image)

**Figure 3.6:** (a) Conductance correction of the AlN/SiO$_2$ sample; (b) Conductance correction of the Al$_2$O$_3$ sample

![Graph showing conductance correction of the B6 sample.](image)

**Figure 3.7:** Conductance correction of the B6 sample
3. Results and Discussion

Figure 3.8: Conductance correction of the F2 sample

Figure 3.9: Conductance correction of the SiO$_2$ sample annealed in N$_2$O
3.2. Results from GV data

**Figure 3.10:** Conductance correction of the SiO$_2$ sample grown in the presence of Na.

**Figure 3.11:** Experimental data with model fitted of sample B6 in high accumulation at a bias voltage of 9 V.
4. Conclusions

The dry oxide has the highest density of interface traps and near-interface traps among the dielectrics investigated in this thesis. This is apparent in the CV spectra as well as in the conductance signal in strong accumulation. The N$_2$O annealed sample has similar D$_{it}$ as the dry oxide but lower N$_{bt}$. The oxide made in the presence of Na has the lowest density of D$_{it}$ and N$_{bt}$ of all samples investigated. Both the AlN/SiO$_2$ stack and Al$_2$O$_3$ have lower D$_{it}$ than the dry oxides but because of high leakage the N$_{bt}$ can’t be determined.

Using the Hi/Lo method to determine the D$_{it}$ at the SiC/dielectric interface has proven to have some limitations when it comes to the shape of the CV curve. Effects from traps with very distinctive energy can shift the higher frequency curve causing an overestimate of the D$_{it}$.

The distributed circuit model shows promise in determining the N$_{bt}$ in the dielectric close to the interface. As with the Hi/Lo method the model has a limitations. The GV spectra has to be well behaved in strong accumulation to extract the series resistance and make the correction to the GV spectra. Using the admittance equation the fit is not perfect and in [24] a modification has been made to equation 2.7 and is claimed to give better fit. Exploring the modification to the distributed circuit model is a topic for future work.
Bibliography


A. Appendix

A.1. Matlab code for CV calculations

clear all
close all

%% File and temperature

% sample name = 'F2';
% T = [77,100,150,200,250,298,350,400]; % temperature [K]
% fileID = {'F2−300um−77K−03−01','F2−300um−100K−03−01','F2−300um−150K−03−01','F2−300um−200K−03−01','F2−300um−250K−03−01','F2−300um−298K−03−06','F2−300um−350K−03−01','F2−300um−400K−03−01'};

% sample name = 'B6';
% T = [77,100,125,150,200,250,298]; % temperature [K]
% fileID = {'B6−300um−03−77K−01','B6−300um−03−100K−01','B6−300um−03−125K−02','B6−300um−03−150K−01','B6−300um−03−200K−01','B6−300um−03−250K−01','B6−300um−03−298K−01'};

% sample name = 'B6';
% T = 298;
% fileID = {'B6−300um−298K−04−02'};

% sample name = 'Al2O3';
% T = [100,300];
% fileID = {'Al2O3−100K−300um.xlsx','Al2O3−300K−300um.xlsx'};
% sample_name = 'AlN–SiO2';
T = [77, 298];

% sample_name = 'F2';
T = [77, 298];
fileID = {'F2–298K–300um–05–01.xlsx', 'F2–77K–300um–05–01.xlsx'};

D_E = cell(1, length(T));
Dit = cell(1, length(T));

%% Constants related to the dialectic
phi_m = 4.26; % metal workfunction [eV]
e_ox = 3.6; % oxide permittivity factor
sigma = 1.5e−19; % cross section [m^2]
r = 150e−6; % pad radius [m]

for l = 1: length(T)
  % Constants defined
  k = 1.38064852e−23; % Boltzmann constant [m^2*kg*s^−2*K^−1]
e_vac = 8.854e−12; % permittivity of vacuum [s^4*A^2*m^−3*kg^−1]
e_semi = 9.66; % semiconductor permittivity factor
q = 1.602e−19; % elementary charge [coulumb]
m_e = 9.11e−31; % electron mass [kg]
h = 6.626e−34; % Planck’s constant [m^2*kg*s^−1]
E_g = 3.3; % semiconductor energy gap [eV]
A = pi*r^2; % pad area [m^2]
X_s = 3.6; % semiconductor workfunction [eV]

  % Effective DOS and thermal velocity calculated
  N_c = 2*((2*pi*0.45*m_e*k*T(l))/(h^2))^(3/2); % Effective DOS in conduction band
  N_v = 2*((2*pi*0.66*m_e*k*T(l))/(h^2))^(3/2); % Effective DOS in valence band
  n_i = sqrt(N_c*N_v)*exp(-(q*E_g)/(2*k*T(l))); % Intrinsic carrier density
  v_th = sqrt((3*k*T(l))/(m_e)); % Thermal velocity [m/s]

  % Data from file extracted
  file_content = importdata(char(fileID(l)));
  BIAS = file_content.data(:,1);
  size = size(file_content.data);
A.1. Matlab code for CV calculations

```matlab
j = 1;
for i = 2:3:size(2)
    frequency(j) = file_content.data(1,i);
    C(:,j) = file_content.data(:,i+1);
    G(:,j) = file_content.data(:,i+2);
    j = j+1;
end

%% Sorting Frequency, C and G
freq = sort(frequency);
for i = 1:length(freq)
    [freq,f_index] = min(abs(frequency-freq(i)));
    cap(:,i) = C(:,f_index);
    cond(:,i) = G(:,f_index).*freq(i);
end
[f_min,f_min_index] = min(freq);
[f_max,f_max_index] = max(freq);
c_geyma{:,1} = num2cell(cap(:,f_max_index));
BIAS_geyma{:,1} = num2cell(BIAS);
e_m = 2*pi.*freq; % Emission rate

%% Doner density calculated
cap_square = (1./cap).^2;
interval = 1:31;
fit_freq = 3;
p = polyfit(BIAS(interval),cap_square(interval,fit_freq),1);
gamma = abs(p(1));
N_D = (2/(q*e_vac*e_semi*A^2*gamma));

%% Oxide capacitance, oxide thickness, Debye length and flatband capacitance calculated and flatband voltage extracted from data
C_ox(1) = mean(max(cap));
t_ox(1) = e_vac*e_ox*(A/C_ox(1));
L_D = sqrt((k*T(1)*e_vac*e_semi)/(q^2*N_D));
C_FB(1) = (e_ox*e_vac)/(t_ox(1)+(e_ox/e_semi*L_D))*A;
C_it = (1./cap(:,f_min_index)-1/C_ox(1)).^(-1)-(1./cap(:,f_max_index)-1/C_ox(1)).^(-1);
phi_ms = phi_m-X_s+E_g/2-k*T(1)/q*log(N_D/n_i);
[c, index_c] = min(abs(cap-C_FB(1)));
V_FB = BIAS(index_c(f_max_index));
N_oc = C_ox(1)*(V_FB-phi_ms)/q;

%% Density of interface states calculated
```

A. Appendix

\[ C_{lf} = \text{cap}(::, f_{\text{min\_index}}); \]
\[ C_{hf} = \text{cap}(::, f_{\text{max\_index}}); \]
\[ D_{it} = 1e4 \times \left( C_{ox(l)} / q \right) \times \left( (C_{lf}/C_{ox(l)} - C_{hf}/C_{ox(l)}) / ((1 - C_{lf}/C_{ox(l)}) \times (1 - C_{hf}/C_{ox(l)})) \right); \]
\[
\%
\text{Theoretical calculation of the CV curve}
\]
\[ psi_s = \text{linspace}(-1, 0.5, 10001); \]
\[ phi_t = kT(l) / q; \]
\[ C_s = (-\text{sign}(psi_s) \times \text{sqrt}((q \times e_{\text{semi}} \times e_{\text{vac}} \times N_D) / 2) \times (1 - \exp(psi_s / phi_t)) \times (\text{sqrt}(phi_t \times \exp(psi_s / phi_t) - psi_s - phi_t))) \times A; \]
\[ CV = (1/C_{ox(l)} + 1. / C_s)^{-1}; \]
\[
\%
\text{Calculating band bending}
\]
\[ \text{for} \ n = 1: \text{length}(BIAS) \]
\[ \quad [y, \text{index\_y}] = \text{min(abs(cap(n, f\_max\_index) - CV))}; \]
\[ \quad phi_{sv}(n) = psi_s(index\_y); \]
\[ \quad C_{m\_nn}(n) = y; \]
\[ \text{end} \]
\[
\%
\text{Calculating Delta E (E_{c-E})}
\]
\[ E_F = kT(l) / q \times \text{log}(N_D / N_c); \]
\[ \text{Delta\_E} = E_F - phi_{sv}'; \]
\[
\%
\text{Finding energy interval}
\]
\[ fasti = N_c \times v_{\text{th}} \times \sigma; \]
\[ \text{for} \ j = 1: \text{length}(freq) \%
\text{Frequency value}
\[ D_{E\_interval}(j) = (-kT(1) \times \text{log}((e_m(j)) / (fasti))) / q; \]
\[ \text{end} \]
\[ [E_{h}, \text{index\_E\_h}] = \text{min(abs(Delta\_E - D\_E\_interval(4)))}; \]
\[ [E_{l}, \text{index\_E\_l}] = \text{min(abs(Delta\_E - D\_E\_interval(1)))}; \]
\[ E = \text{Delta\_E(index\_E\_l:index\_E\_h)}; \]
\[ D = D_{it}(index\_E\_l:index\_E\_h); \]
\[
\%
\text{Plotting graphs}
\]
\[ \text{figure(1)} \]
\[ \text{subplot(2,2,1)} \]
\[ \text{plot(BIAS, cap(::, f\_max\_index))} \]
\[ \text{xlabel('BIAS [V]'') } \]
\[ \text{ylabel('Capasitance [F]'') } \]
A.1. Matlab code for CV calculations

```matlab
subplot(2,2,2)
plot(psi_s,CV)
xlabel(’\phi_{s} [eV]’)
ylabel(’Capasitance [F]’)

subplot(2,2,3)
plot(BIAS,phi_sv)
xlabel(’BIAS [V]’)
ylabel(’\phi_{s} [eV]’)

subplot(2,2,4)
plot(psi_s,psi_s)
xlabel(’\phi_{s} [eV]’)
ylabel(’\phi_{s} [eV]’)

%% Extracting D_{it} and Delta E
D_E{l} = num2cell(Delta_E(index_E_l:index_E_h)) ;
Dit{l} = num2cell(D_it(index_E_l:index_E_h)) ;

% Clear cells
clear size
clear file_content
clear C
clear G
clear cap
clear cond
clear phi_sv
end

figure(1+1)
for h = 1:length(T)
    plot(cell2mat(D_E{1,h}),cell2mat(Dit{1,h}),'—*','DisplayName',['T = ',num2str(T(h)),' K'])
    legend(’—DynamicLegend’);
    hold on
end
xlabel(’\DeltaE [eV]’)
ylabel(’D_{it} [cm^{-2} eV^{-1}]’)

figure(1+2)
for h = 1:length(T)
    plot(cell2mat(BIAS_geyma{: ,h}),cell2mat(c_geyma{: ,h})*1e12,....
end
```
A. Appendix

```matlab
A.2. Matlab code for GV calculations

cle
clear all
close all

%% Constants related to the dialectric and the sample
sigma = 1.5e-19; % cross section [m^2]
A = pi*0.015^2; % Area of MOS capacitor [cm^2]
e_ox = 3.6; % oxide permittivity factor
tox = 3.5317e-06; % Oxide thinckness [cm]
Dit = 2.307e12 ; % Density of interface states [cm^-2 eV^-1]
Cox = 6.611e-11/A; % [F/cm^2]
Cd = 6e-5; % [F/cm^2]
k0 = 8.819560455152439e+06; % cm^-1, kappa – decay factor
t0 = 7.635484417274337e-12; % [s]

V_intrerest = 7;

%% Defining constants
q = 1.602e-19; % elementary charge [coulombs]
h = 6.626e-34; % Planck’s constant [m^2*kg*s^-1]
h_bar = h/(2*pi);% [eV*s*rad^-1]
m_e = 9.109e-31; % electron mass [kg]
k = 1.38064852e-23; % Boltzmann constant [m^-2*kg*cm^2*s^-2*K^-1]
e_vac = 8.854e-12; % permittivity of vacuum [s^-4*A^-2*m^-3*kg^-1]
e_semi = 9.66*e_vac; % semiconductor permittivity factor

%% File and temperature
% sample_name = 'B6';
% T = 298; % temperature [K]
% fileID = {'B6−300um−298K−04−02'};
```
sample_name = 'F2';
T = 295;
fileID = {'F2-298K-300um-05-01'};

% sample_name = 'Al2O3';
% T = 300;
% fileID = {'Al2O3-300K-300um.xlsx'};

% sample_name = 'Al2O3';
% T = 298;
% fileID = {'AlN-SiO2-300um-298K.xlsx'};

% sample_name = 'F2';
% T = 298; % temperature [K]
% fileID = {'F2-298K-300um-04-01'};

% Data from file extracted
for l = 1:length(T)
    file_content = importdata(char(fileID(l)));
    BIAS = file_content.data(:,1);
    size = size(file_content.data);
    j = 1;

    for u = 2:3:size(2)
        freq(j) = file_content.data(1,u);
        cap(:,j,1) = file_content.data(:,u+1);
        cond(:,j,1) = file_content.data(:,u+2);
        j = j+1;
    end
    clear size
    clear file_content
end

% Sorting Frequency, C and G
frequency = sort(freq);
for u = 1:length(freq)
    [frequ,f_index] = min(abs(freq-frequency(u)));
    C(:,u) = cap(:,f_index);
    G(:,u) = cond(:,f_index).*frequency(u);
end

% Conductance correction
[V, V_index] = min(abs(V_interest-BIAS)); % Voltage of interest
77 \( w = 2\pi \times \text{frequency}; \)
78 Deil = G(V_{index} ,:)/(w.*C(V_{index} ,:).^2);
79 p = polyfit(w(18:28),Deil(18:28),1);
80 R_s = p(1);
81 a = G - (G.^2 + w.^2.*C.^2).*R_s;
82 G_c = ((G.^2 + w.^2.*C.^2).*a)./(a.^2 + w.^2.*C.^2);
83 C_c = (G.^2 + w.^2.*C.^2).*C./(a.^2 + w.^2.*C.^2);
84
85 \% Near interface traps calculations
86 tn = t0; \% [s]
87 Nox = 2000;
88 Coxn = Cox*Nox;
89 N_add = 0;
90 o = 1;
91 G_max = zeros;
92 G_max(1) = 1;
93 G_max(2) = 0.5;
94 Nbt = 1e14; \% cm^{-3}, bulk-oxide trap density
95
96 while G_max(o) > G_max(o+1)
97 Nbt = Nbt + N_add;
98 G_tot = zeros(1,length(w));
99 C_tot = zeros(1,length(w));
100 for u = 1:length(w)
101 \% CTn, , Ggr and Ybt defined in Chapters 3 and 4
102 F = @(f)(1-f)/((1+j*w(u)*f.*(1-f)+(1-f))./tn);
103 [Hcn, errbnd] = quadgk(F,0,1,'RelTol',1e-10);
104 CTn=(q*Dit*Hcn)/tn;
105 F = @(f)1./(1+j*w(u)*f.*(1-f)+(1-f)./tn);
106 [Hg, errbnd] = quadgk(F,0,1,'RelTol',1e-10);
107 Ggr=(q*Dit*Hg)/tn;
108 Y=1j*w(u)*(Cd+CTn)+Ggr;
109 for v = 1:Nox
110 Cpbtl=q/w(u)*t0*(Nbt*atan(w(u)*t0*exp(2*k0*tox/Nox*(v-1)))/... exp(2*k0*tox/Nox*(v-1))+Nbt*atan(w(u)*t0*exp(2*k0*tox/... Nox*(v)))/exp(2*k0*tox/Nox*(v)))*tox/Nox/2;
111 Gpbtl=q/2/t0*(Nbt*log(1+w(u)^2*t0^2*exp(4*k0*tox/Nox*(v-1)))/... exp(2*k0*tox/Nox*(v-1))+Nbt*log(1+w(u)^2*t0^2*...
A.2. Matlab code for GV calculations

```matlab
exp(4*k0*...
tox/Nox*(v)))/exp(2*k0*tox/Nox*(v))*tox/Nox/2;
Ypbt=1j*w(u)*Cpbt+Gpbt;
Y=1j*w(u)*Coxn*Y/(1j*w(u)*Coxn+Y)+Ypbt;

end
G_tot(u)=real(Y);
C_tot(u)=imag(Y)/w(u);

G_max(o+2) = max(max(abs(G_c(V_index,:) ./A−G_tot)));
N_add = 1e12 * o;
o = o + 1;
end
Nbt = Nbt*2e−7;

%% plotting figures
figure (1)
plot (BIAS,C_c)
xlabel ( 'BIAS [V] ')
ylabel ( 'Capasitance [F] ')

figure (2)
subplot (2,1,1)
plot (BIAS,G)
xlabel ( 'BIAS [V] ')
ylabel ( 'Conductance [S] ')
subplot (2,1,2)
plot (BIAS,G_c)
xlabel ( 'BIAS [V] ')
ylabel ( 'Conductance [S] ')

figure (3)
subplot (2,1,1)
plot (frequency,G_c(V_index,:)/A, '−' )
hold on
plot (frequency,G_tot, 'k')
xlabel ( 'Frequency [rad/s] ')
ylabel ( 'Conductance [S/cm^2] ')
subplot (2,1,2)
plot (frequency,C_c(V_index,:)/A, '−' )
hold on
plot (frequency,C_tot, 'k')
```

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A. Appendix

161 \texttt{xlabel(’Frequency [rad/s]’)}

162 \texttt{ylabel(’Conductance [F/cm^2]’)}